

# Compal Confidential

## Lotus M/B Schematics Document

14": Elise; 15.6" Exige

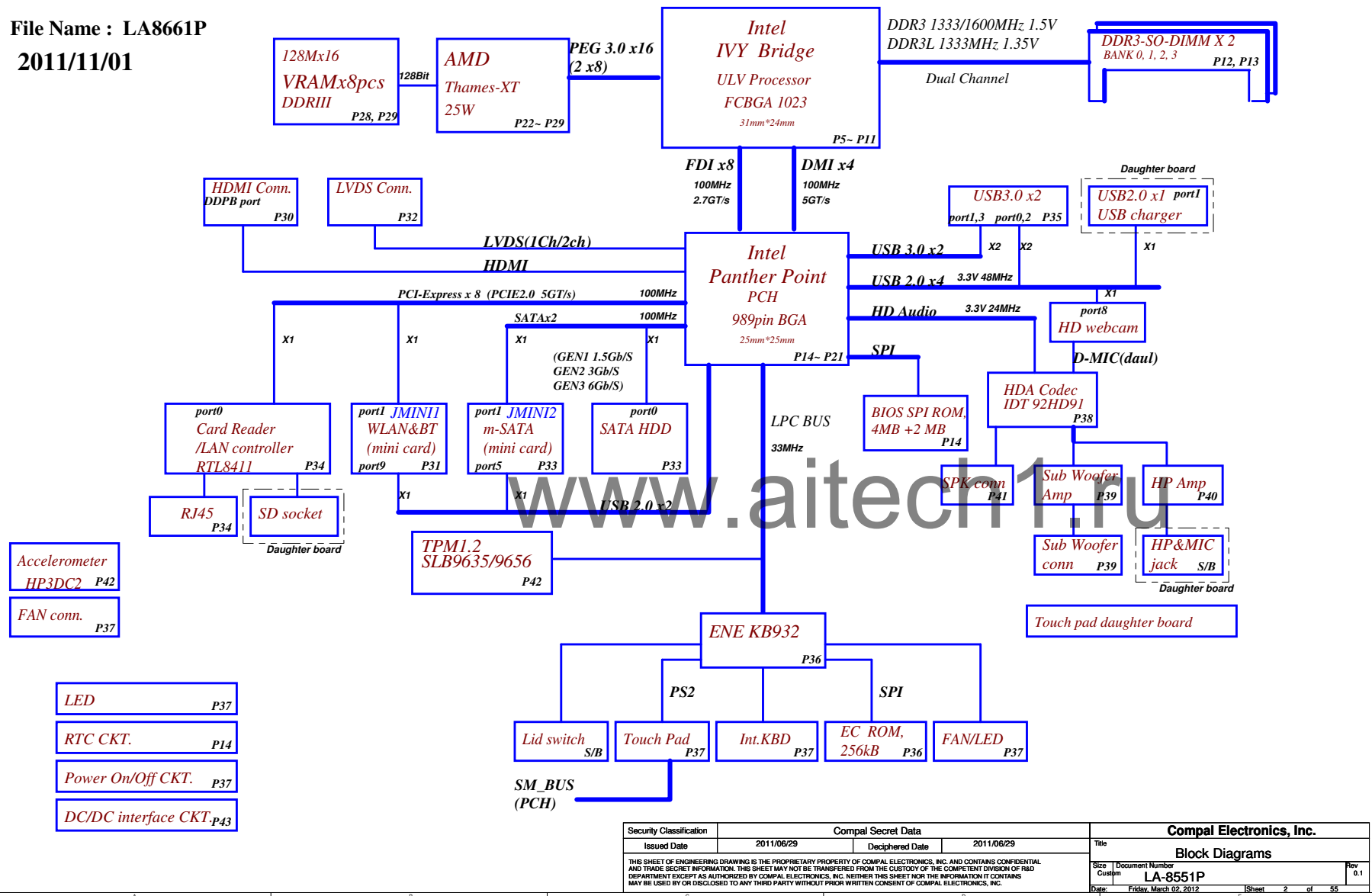
Intel Ivy Bridge ULV Processor with DDRIII + Panther Point

Date : 2011/10/27

Version 0.1

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	
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				Rev	0.1

**2011/11/01**



# QAU30/50 (LA-8661P Ver:0.1)

## Volatge Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
		ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V ) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+SVALW ) to 1.8V switched power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON
+3VALW_EC	+3VALW always to KBC	ON	ON	ON
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+SVALW	+SVALWP to +SVALW power rail	ON	ON	ON
+5V_PCH	+SVALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON
+5VS	+SVALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Power Plane	Description	S1	S3	S5
+VGA_CORE	GPU power	PX	OFF	OFF
+3VGS	GPU power	PX	OFF	OFF
+1.8VGS	GPU power	PX	OFF	OFF
+1.5VGS	GPU power	PX	OFF	OFF
+1.0VGS	GPU power	PX	OFF	OFF

## EC SM Bus1 address

Device	Address
Smart Battery	
G-sensor	0x50/0x52

## PCH SM Bus address

Device	Address
DDR DIMM0	
DDR DIMM1	
Mini Card1	
Mini Card2	
TP module	



## EC SM Bus2 address

Device	Address
PCH (Reserve)	

SMBUS Control Table

	SOURCE	BATT	WLAN MIINI1	BATT Charger	TP	SODIMM	EC_SMB_CRK2 EC_SMB_DA2	PCH_SML1CLK PCH_SML1DATA	G-Sensor	GPU	HP AMP
EC_SMB_CRK1 EC_SMB_DA1	KB930	V		V					V		
EC_SMB_CRK2 EC_SMB_DA2	KB930							V		V	V
PCH_SMBCLK PCH_SMBDATA	PCH		@		V	V					
PCH_SML0CLK PCH_SML0DATA	PCH										
PCH_SML1CLK PCH_SML1DATA	PCH						V				

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	PCIE LAN CARD READER	CLKOUTFLEX0	None
			CLKOUTFLEX1	None
	CLKOUT_PCIE1	mini WLAN	CLKOUTFLEX2	None
	CLKOUT_PCIE2	None	CLKOUTFLEX3	DGPU_PRSENT#
	CLKOUT_PCIE3	None		
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :  
 : means Digital Ground  
 : means Analog Ground

Project ID	30UMA@	30DIS@	50UMA@	50DIS@
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PCB	LA-8661P	LA-8662P
	PX@	UMA@

BY SKU			
TPM	9635@	9656@	
CPU	CPUUMA1@	CPUUMA2@	CPUDIS@
VRAM	X76@	H2G@	M2G@ S2G@

Option	@	CONN@	USB30@	PX@	UMA@	DIS@	THA@
UMA	X	X	V	X	V	X	X
DIS	X	X	V	V	X	V	V

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC
PCI2	None
PCI3	None
PCI4	None

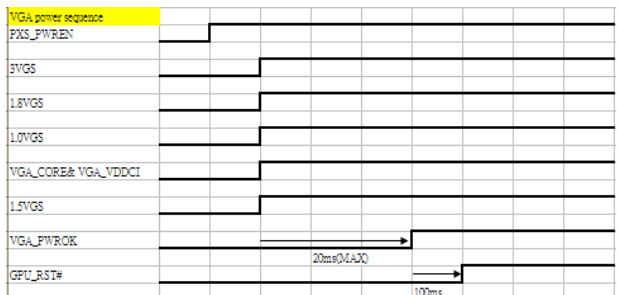
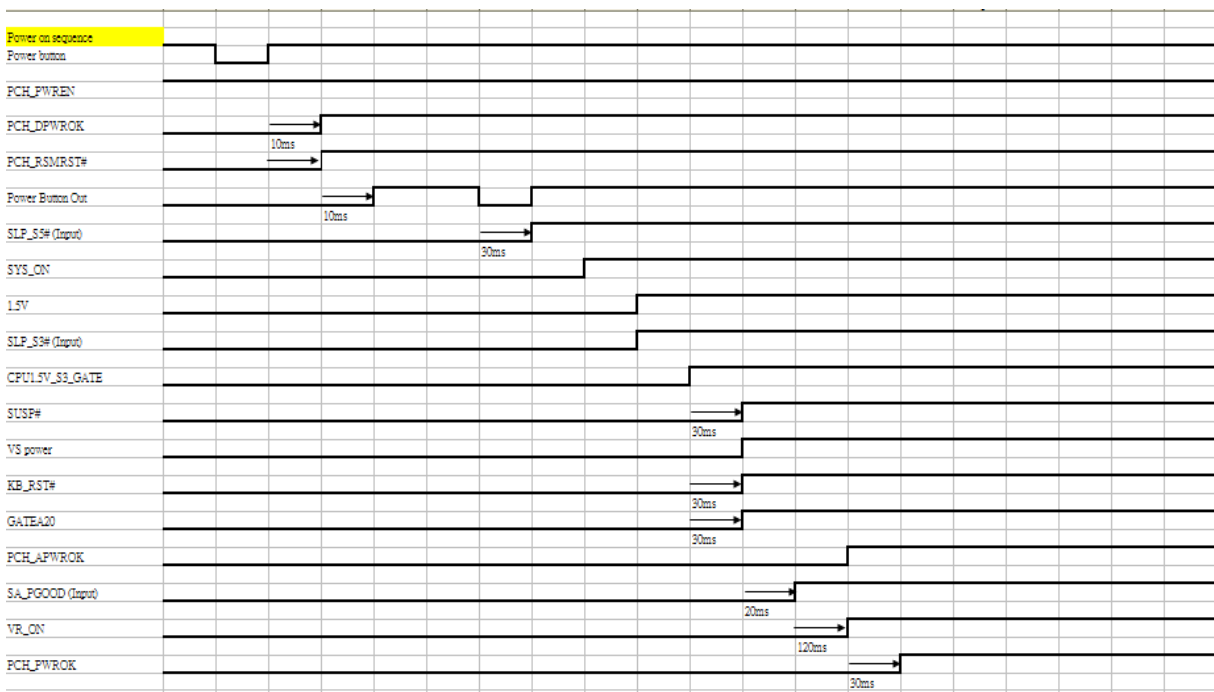
SATA	DESTINATION
SATA0	SATA, JHDD1
SATA1	m-SATA,JMINI2
SATA2	None
SATA3	None
SATA4	None
SATA5	None

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB2.0 (left Side)
		1	USB2.0 (right Side)
		2	USB2.0 (left Side)
	UHCI2	3	None
		4	None
		5	None
		6	None
UHCI3	7	None	
	8	Camera	
EHCI2	UHCI4	9	Mini Card(WLAN& BT)
		10	None
	UHCI5	11	None
		12	None
		13	None

USB 3.0	Port	2 External USB Port
	1	USB3.0 (left Side)
	2	None
	3	USB3.0 (left Side)
	4	None

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UCPU1 CPUIDIS01@  
I5-2467M CPU  
SA00004X000

UCPU1 CPUIDIS02@  
I5-2367M CPU  
SA000051H20

UCPU1 CPUIDIS03@  
I5-2367M CPU  
SA000051H20

UCPU1 CPUIDIS04@  
I5-3317U CPU  
SA00005K600

UCPU1 CPUUMA3@  
I5-2367M CPU  
SA000051H20

UCPU1 CPUUMA4@  
17W 1.7GHz GT2 ES2 QBP7  
SA00005B010

UCPU1 CPUUMA5@  
17W 1.7GHz no only ES2 QBTQ  
SA00005B020

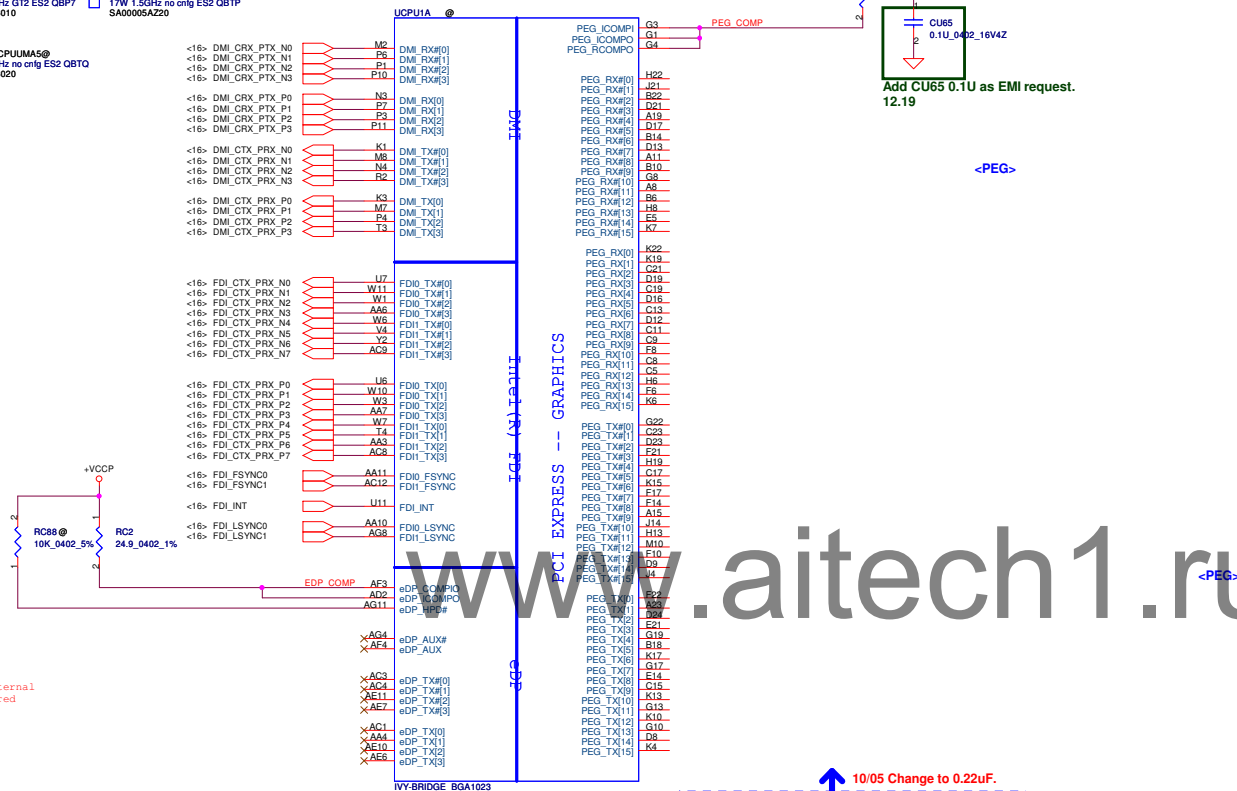
UCPU1 CPUUMA1@  
17W 1.5GHz GT2 ES2 QBP8  
SA00005AZ10

UCPU1 CPUUMA2@  
17W 1.5GHz no only ES2 QBTQ  
SA00005AZ20

Sandy Bridge:  
Intel Core I5-2467M: SA00004X000 (4619HY32L01)

Ivy Bridge:  
1.5GHz GT2 ES2 QBP8: SA00005AZ10 (4619HZ32L01)  
1.5GHz ES2 QBTQ: SA00005AZ20 (4619HZ32L02)

PEG\_ICOMPI and RCOMPO signals should be  
shorted and routed  
with - max length = 500 mils - typical  
impedance = 43 mohms  
PEG\_ICOMPO signals should be routed with -  
max length = 500 mils  
- typical impedance = 14.5 mohms



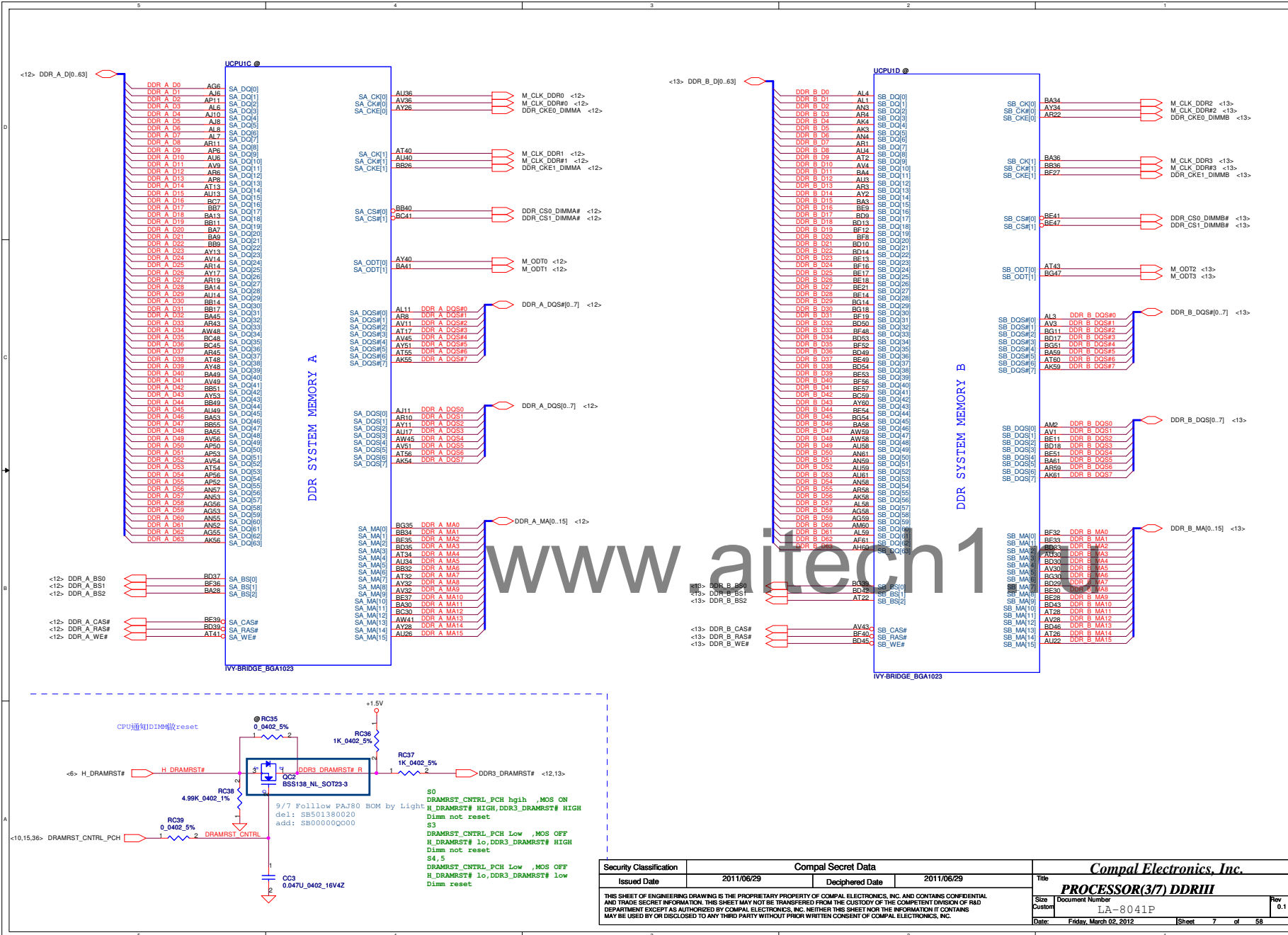
eDP\_COMPIO and ICOMPO signals  
should be shorted near balls  
and routed with typical  
impedance <25 mohms

NOTE: eDP\_COMPIO and eDP\_ICOMPO  
should not be left floating even if Internal  
Graphic is disabled since they are shared  
with other interfaces

Typ- suggest 220nF. The change in AC capacitor  
value from 180nF to 265nF is to enable  
compatibility with future platforms having PCIe  
Gen3 (8GT/s)

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				PROCESSOR(I7) DMI,FDI,PEG	
Size		Document Number		Rev	
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Date:		Friday, March 02, 2012		Sheet 5 of 58	

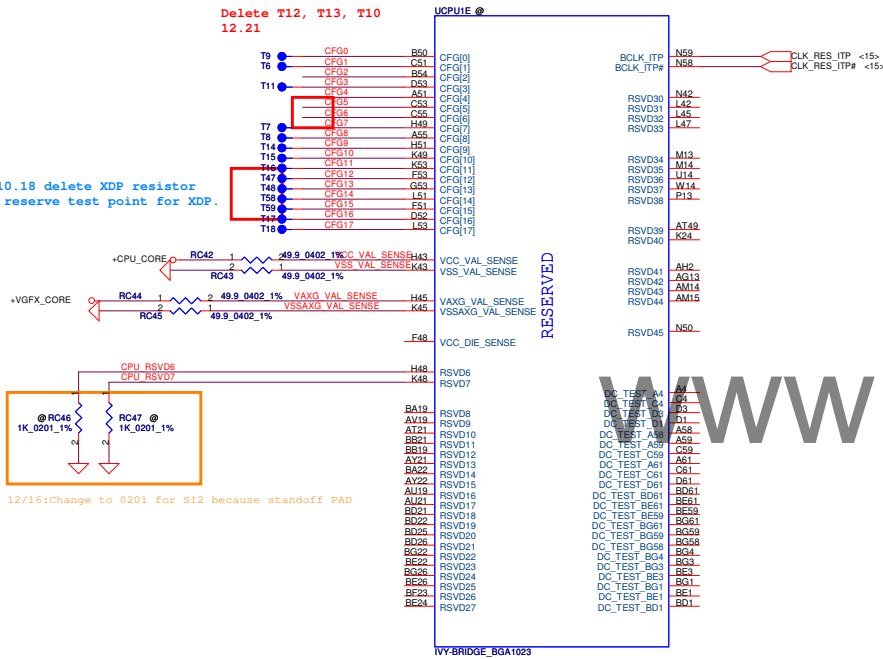




Change to part G.

Delete T12, T13, T10  
12.21

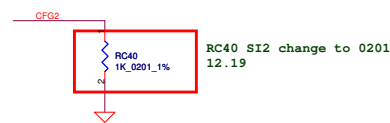
2011.10.18 delete XDP resistor  
just reserve test point for XDP.



## CFG Straps for Processor

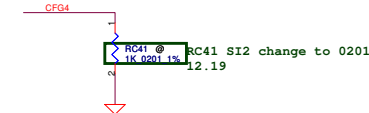
PEG bus is reversed, need to PD.

11.01



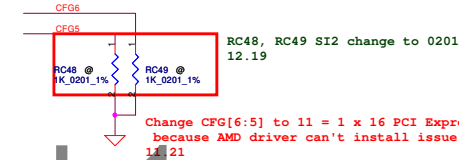
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	<ul style="list-style-type: none"><li>★ 1: Normal Operation; Lane # definition matches socket pin map definition</li><li>0: Lane Reversed</li></ul>
------	---



Display Port Presence Strap

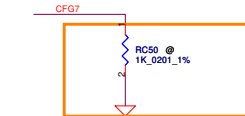
CFG4	<ul style="list-style-type: none"><li>★ 1: Disabled; No Physical Display Port attached to Embedded Display Port</li><li>0: Enabled; An external Display Port device is connected to the Embedded Display Port</li></ul>
------	---



PCIe Port Bifurcation Straps

CFG[6:5]	<ul style="list-style-type: none"><li>00 = 1 x 8, 2 x 4 PCI Express</li><li>01 = reserved</li><li>10 = 2 x 8 PCI Express</li><li>11 = 1 x 16 PCI Express</li></ul>
----------	--

12/16: Change to 0201 for SI2 because standoff PAD



PEG DEFER TRAINING

CFG7	<ul style="list-style-type: none"><li>★ 1: (Default) PEG Train immediately following xxRESETB de assertion</li><li>0: PEG Wait for BIOS for training</li></ul>
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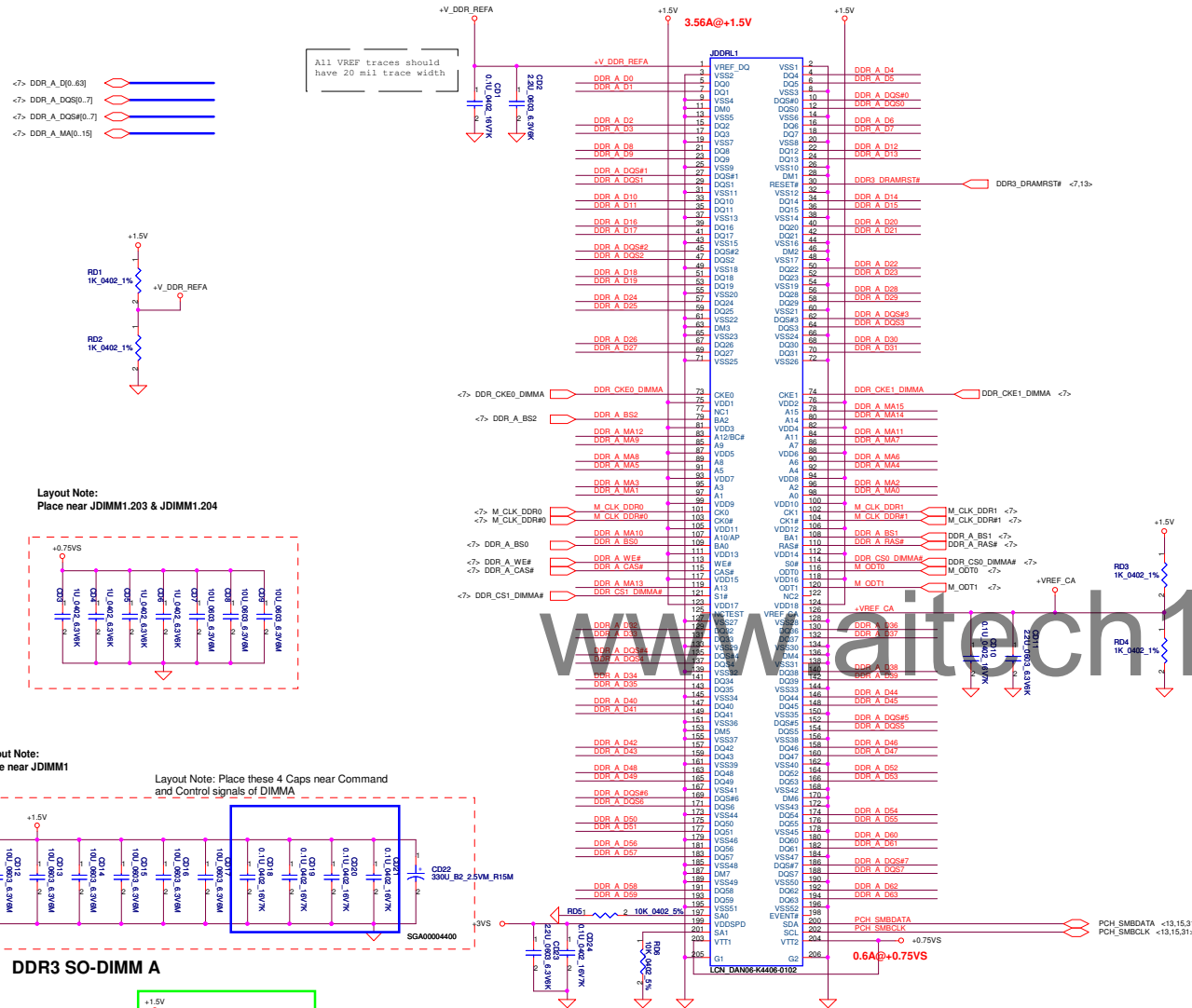






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### DDR3 SO-DIMM A



**Standard**  
**<Address(SA1,SA0):00>**

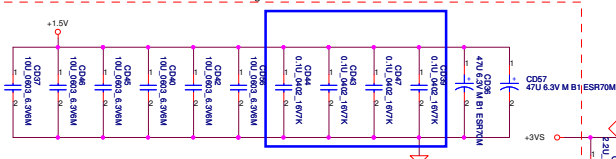
Security Classification		Compel Secret Data		Title	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	<div style="text-align: center;"> <b>DDRIII DIMM</b>  <b>LA-8661P</b> </div>	
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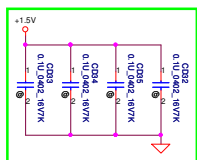
10/03 change to +V\_DDR\_REFB



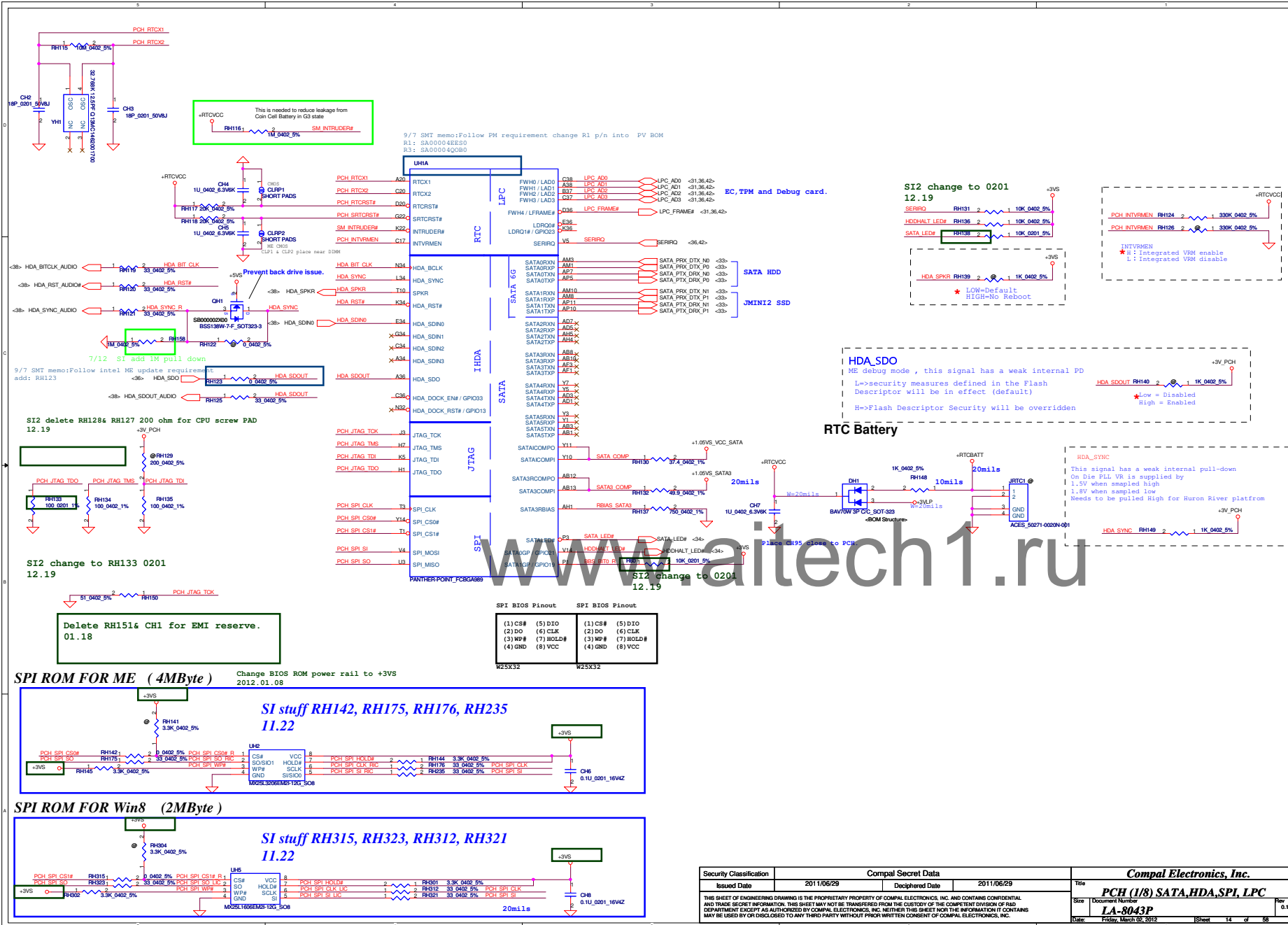
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



10/05 change to PH.

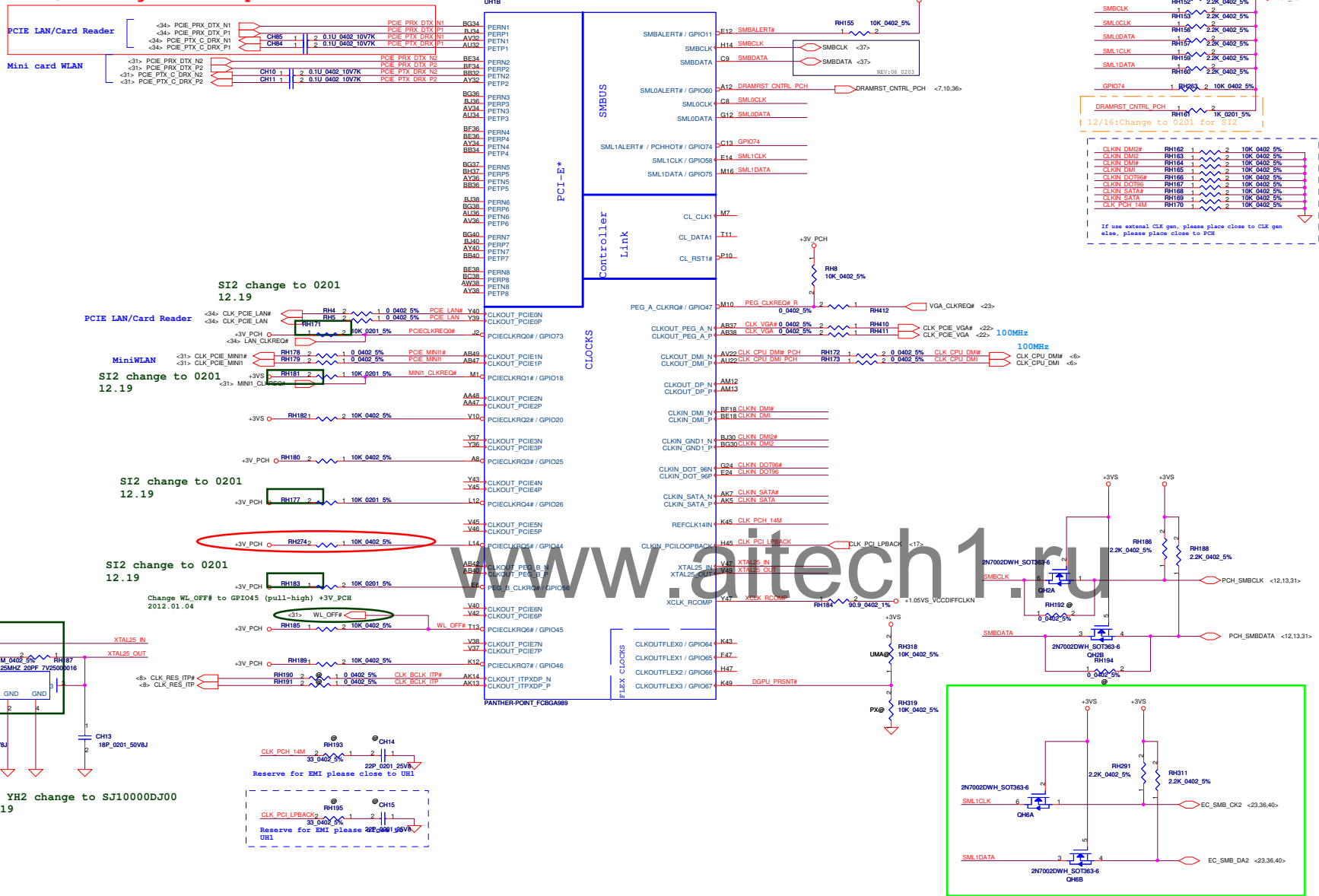


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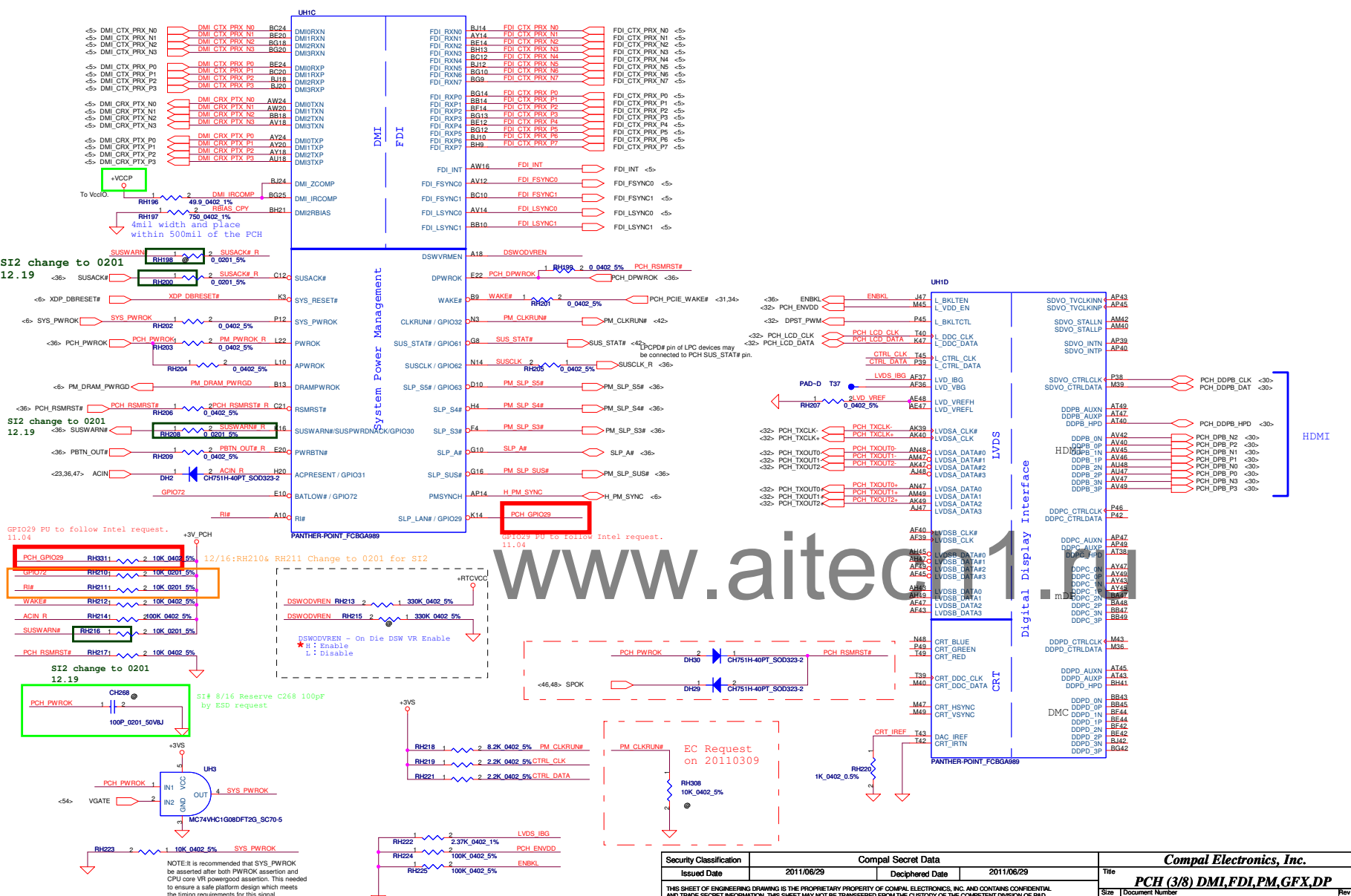


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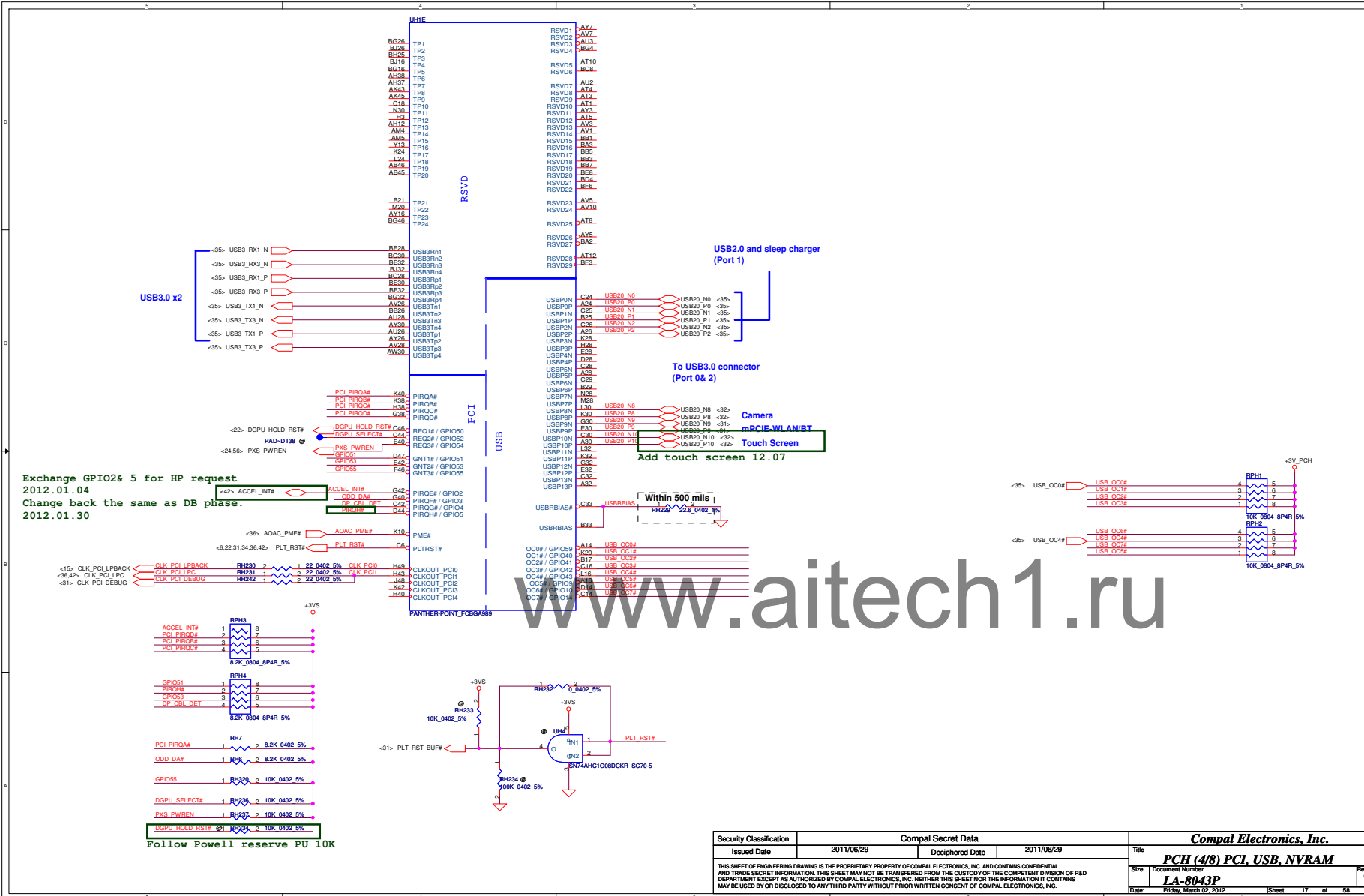
10/03 change to PCIE port1.

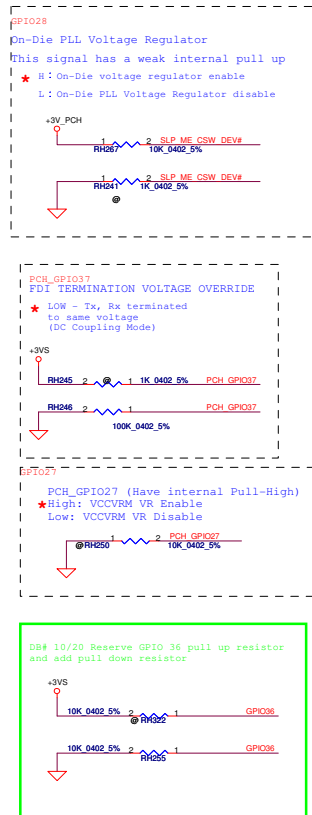


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		Size	Document Number
			LA-8043P
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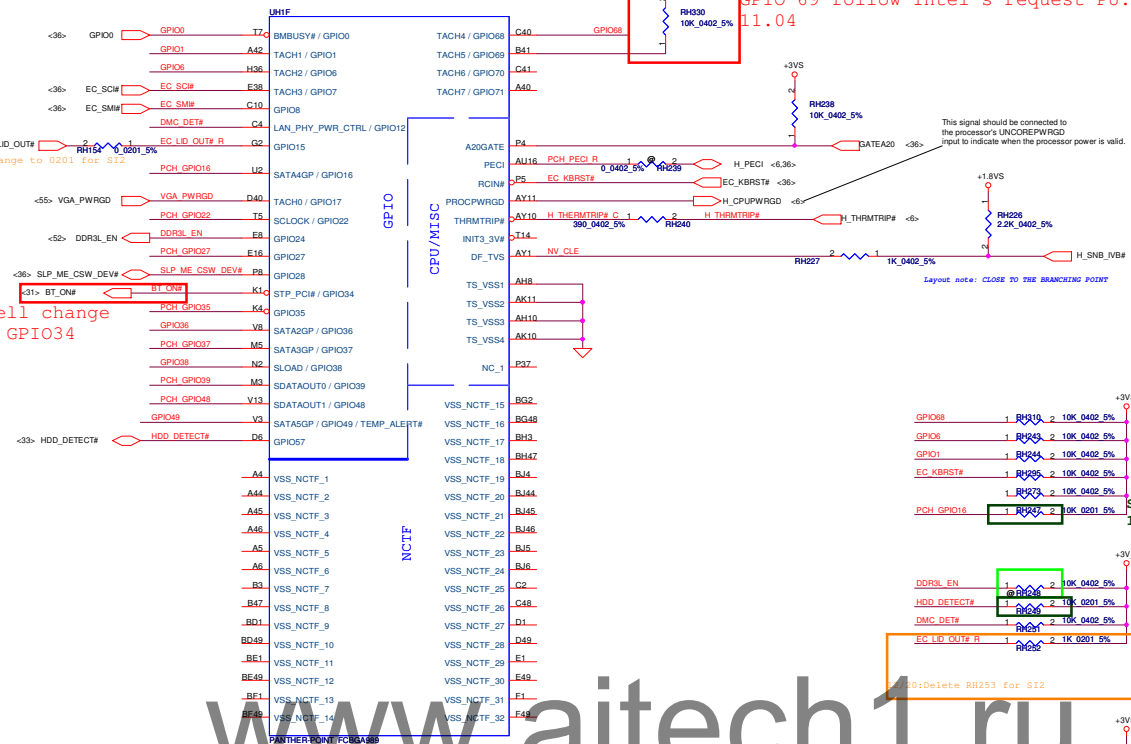


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Refer Powell change  
 BT\_ON to GPIO34  
 10.21



Refer Powell change  
 BT\_ON to GPIO34  
 10.21

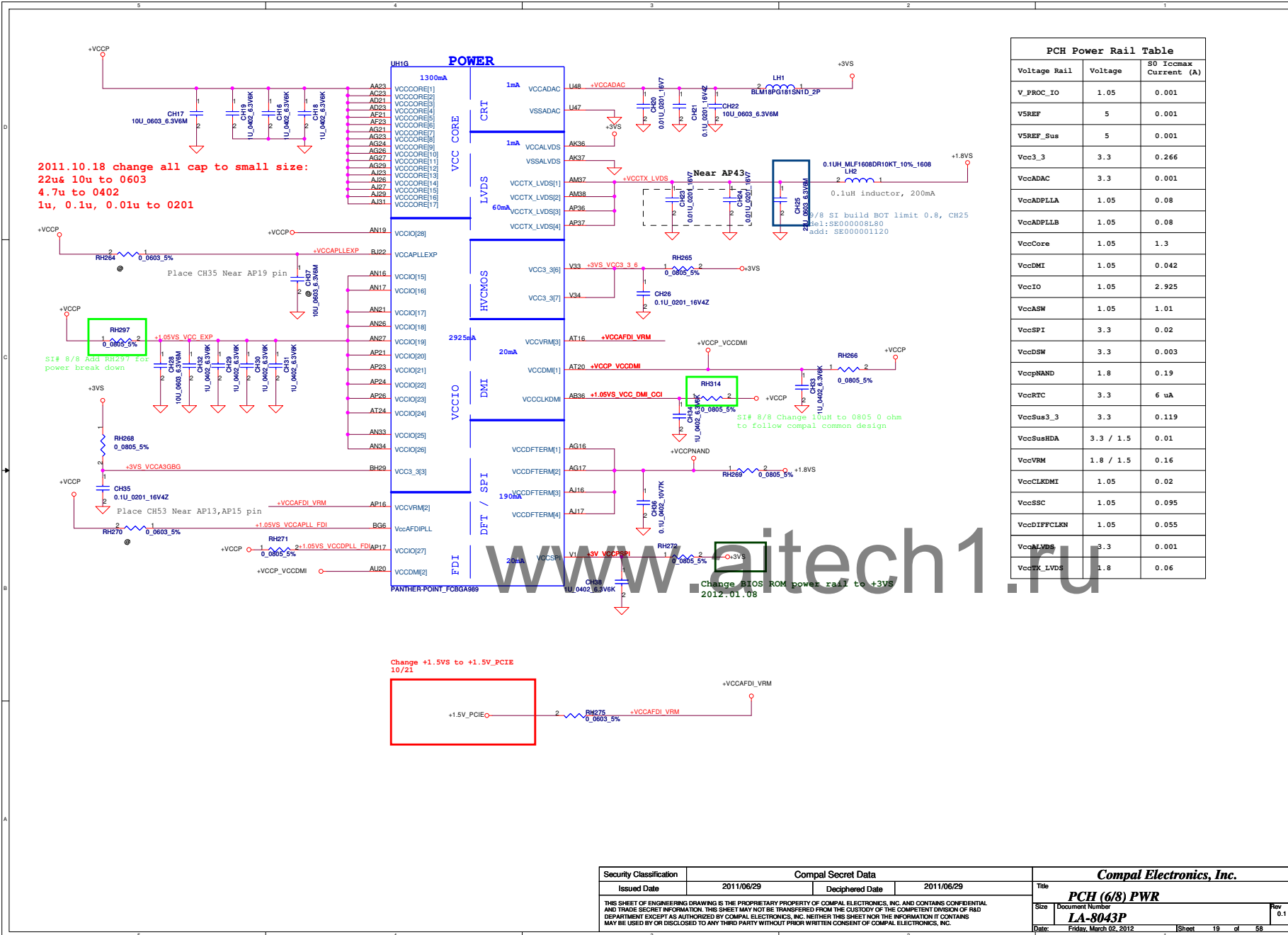
SI# 8/8 change PCH\_WAN\_RADIO\_OFF#  
 to PCH\_GPIO15

SI2 change to 0201  
 12.19

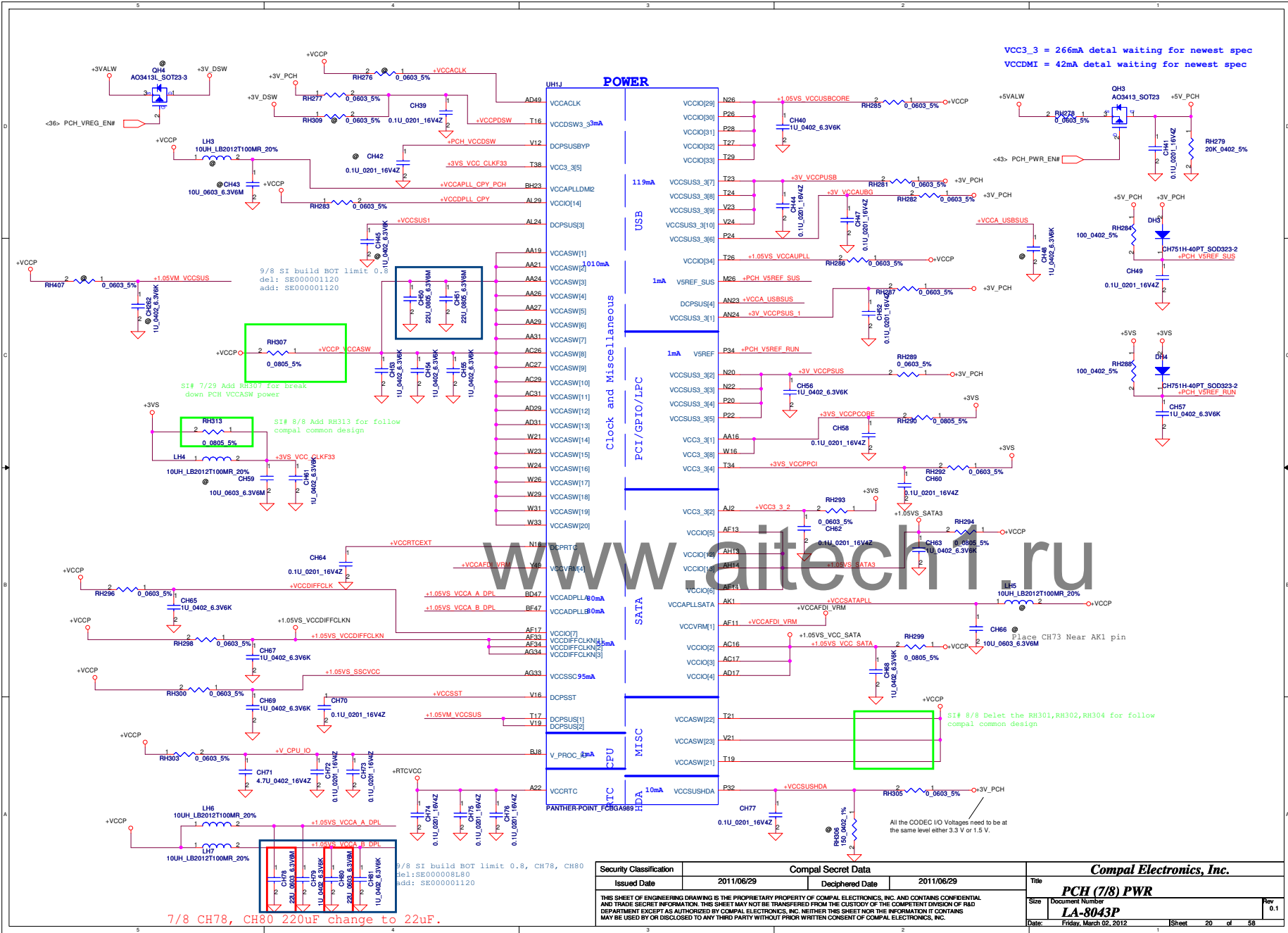
SI2 change to 0201  
 12.19

SI2 change to 0201  
 12.19

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PCH Power Rail Table		
Voltage Rail	Voltage	80 Iccmax Current (A)
V_PROC_IO	1.05	0.001
VSREF	5	0.001
VSREF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADC	3.3	0.001
VccADPLL	1.05	0.08
VccADPLLb	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06





UHH		
H5	VSS[0]	
AA17	VSS[80]	AK38
AA2	VSS[81]	VSS[81]
AA5	VSS[82]	AK42
AA33	VSS[83]	AK46
AB11	VSS[84]	AL16
AB14	VSS[85]	AL17
AB38	VSS[86]	AL2
AB4	VSS[87]	AL21
AB5	VSS[88]	AL23
AB7	VSS[89]	AL26
AC18	VSS[90]	AL27
AC2	VSS[91]	AL31
AC21	VSS[92]	AL33
AC24	VSS[93]	AL34
AC3	VSS[94]	AL48
AC33	VSS[95]	AM11
AC4	VSS[96]	AM14
AC48	VSS[97]	AM36
AD10	VSS[98]	AM39
AD11	VSS[99]	AM43
AD12	VSS[100]	AM45
AD13	VSS[101]	AM46
AD18	VSS[102]	AM7
AD24	VSS[103]	AN2
AD26	VSS[104]	AN29
AD27	VSS[105]	AN3
AD33	VSS[106]	AN31
AD34	VSS[107]	AP12
AD36	VSS[108]	AP19
AD37	VSS[109]	AP28
AD38	VSS[110]	AP30
AD39	VSS[111]	AP32
AD4	VSS[112]	AP38
AD42	VSS[113]	AP4
AD43	VSS[114]	AP42
AD43	VSS[115]	AP46
AD45	VSS[116]	AP5
AD46	VSS[117]	AR2
AD8	VSS[118]	AR46
AE2	VSS[119]	AT11
AE3	VSS[120]	AT13
AE3	VSS[121]	AT22
AE10	VSS[122]	AT26
AE12	VSS[123]	AT28
AD14	VSS[124]	AT30
AD16	VSS[125]	AT32
AE16	VSS[126]	AT34
AE19	VSS[127]	AT39
AE24	VSS[128]	AL42
AE27	VSS[129]	AT46
AE28	VSS[130]	AT7
AE31	VSS[131]	AL24
AE31	VSS[132]	AL30
AE38	VSS[133]	AV16
AE4	VSS[134]	AV20
AE40	VSS[135]	AV24
AE46	VSS[136]	AV30
AE5	VSS[137]	AV38
AE7	VSS[138]	AV4
AF8	VSS[139]	AV43
AG10	VSS[140]	AV9
AG2	VSS[141]	AW14
AG31	VSS[142]	AW18
AG46	VSS[143]	AW2
AH11	VSS[144]	AW22
AH3	VSS[145]	AW28
AH36	VSS[146]	AW32
AH39	VSS[147]	AW36
AH40	VSS[148]	AW40
AH42	VSS[149]	AW46
AH46	VSS[150]	AW5
AH7	VSS[151]	AW36
AJ19	VSS[152]	AW39
AJ21	VSS[153]	AW40
AJ24	VSS[154]	AW46
AJ33	VSS[155]	AV11
AJ34	VSS[156]	AV12
AK12	VSS[157]	AV22
AK3	VSS[158]	AY28

PANTHER-POINT\_FCBGA989

UHH		
H5	VSS[0]	
AY4	VSS[159]	H46
AY42	VSS[160]	K18
AY46	VSS[161]	K26
AY8	VSS[162]	K32
B11	VSS[163]	K46
B15	VSS[164]	K7
B19	VSS[165]	L18
B23	VSS[166]	L2
B27	VSS[167]	L20
B31	VSS[168]	L26
B35	VSS[169]	L28
B39	VSS[170]	L36
B43	VSS[171]	L48
B47	VSS[172]	M12
B51	VSS[173]	M18
B55	VSS[174]	M22
B59	VSS[175]	M24
B63	VSS[176]	M30
B67	VSS[177]	M32
B71	VSS[178]	M34
B75	VSS[179]	M38
B79	VSS[180]	M4
B83	VSS[181]	M42
B87	VSS[182]	M46
B91	VSS[183]	M8
B95	VSS[184]	N18
B99	VSS[185]	N24
BC22	VSS[186]	P30
BC26	VSS[187]	P47
BC30	VSS[188]	P11
BC34	VSS[189]	P18
BC38	VSS[190]	T33
BC42	VSS[191]	P40
BC46	VSS[192]	P43
BD4	VSS[193]	P47
BD8	VSS[194]	P7
BD12	VSS[195]	R2
BD16	VSS[196]	R48
BD20	VSS[197]	T12
BD24	VSS[198]	T31
BD28	VSS[199]	T37
BD32	VSS[200]	T4
BD36	VSS[201]	T46
BD40	VSS[202]	T47
BD44	VSS[203]	T6
BD48	VSS[204]	V11
BD52	VSS[205]	V17
BD56	VSS[206]	V26
BD60	VSS[207]	V27
BD64	VSS[208]	V28
BD68	VSS[209]	V31
BD72	VSS[210]	V36
BD76	VSS[211]	V38
BD80	VSS[212]	V43
BD84	VSS[213]	V7
BD88	VSS[214]	W17
BD92	VSS[215]	W19
BD96	VSS[216]	W2
BD100	VSS[217]	W27
BD104	VSS[218]	W48
BD108	VSS[219]	Y12
BD112	VSS[220]	Y38
BD116	VSS[221]	Y4
BD120	VSS[222]	Y42
BD124	VSS[223]	Y46
BD128	VSS[224]	Y8
BD132	VSS[225]	BC29
BD136	VSS[226]	N24
BD140	VSS[227]	AJ3
BD144	VSS[228]	AD47
BD148	VSS[229]	B43
BD152	VSS[230]	BE10
BD156	VSS[231]	BC41
BD160	VSS[232]	G14
BD164	VSS[233]	H16
BD168	VSS[234]	H36
BD172	VSS[235]	BC22
BD176	VSS[236]	BC24
BD180	VSS[237]	C22
BD184	VSS[238]	AP13
BD188	VSS[239]	M14
BD192	VSS[240]	AP3
BD196	VSS[241]	AP1
BD200	VSS[242]	BE16
BD204	VSS[243]	BC16
BD208	VSS[244]	BC28
BD212	VSS[245]	BU28
BD216	VSS[246]	VSS[352]
BD220	VSS[247]	
BD224	VSS[248]	
BD228	VSS[249]	
BD232	VSS[250]	
BD236	VSS[251]	
BD240	VSS[252]	
BD244	VSS[253]	
BD248	VSS[254]	
BD252	VSS[255]	
BD256	VSS[256]	
BD260	VSS[257]	
BD264	VSS[258]	

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				Rev	0.1

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				Date:	Friday, March 02, 2012	Sheet 27 of 58

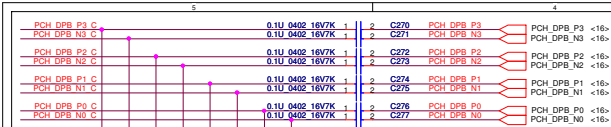
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				Date:	Friday, March 02, 2012	Sheet 28 of 58

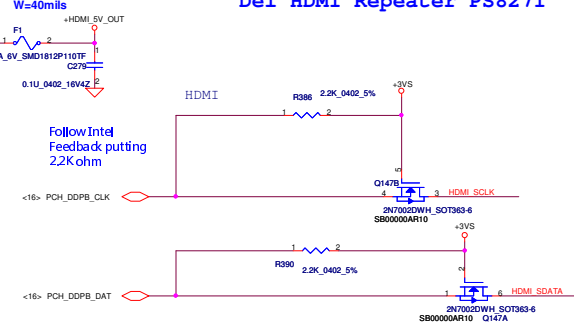


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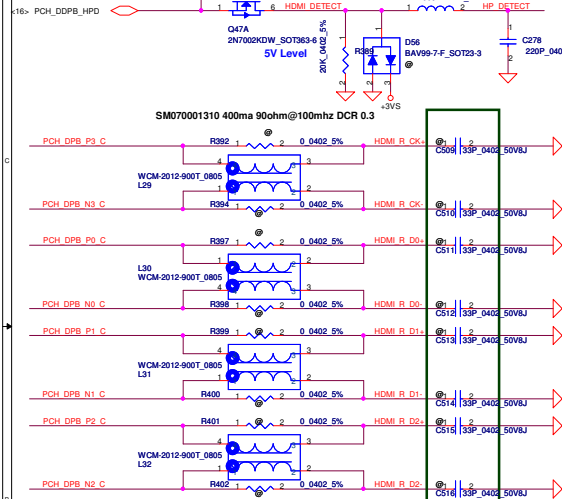
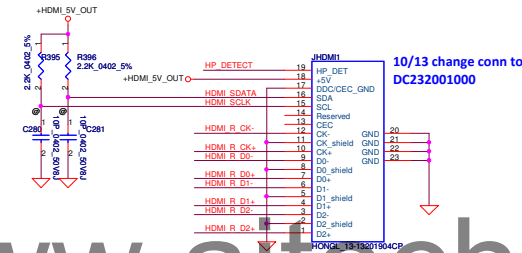
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Issued Date	2011/06/30	Deciphered Date	2013/06/30	Title	ATI SeymourXT M2 VRAM B	
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## Del HDMI Repeater PS8271



## 5V PULL UP IN CONNECTER SIDE



Follow EMI request add 33pF cap to GND.  
11.02

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R73 pull high, and stuff R100  
12.07

WLAN

WL\_OFF# Change from PCH GPIO55 to GPIO46.  
(pull-high change from +3VS to +3V\_PCH)  
12.07

For Wireless LAN

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Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

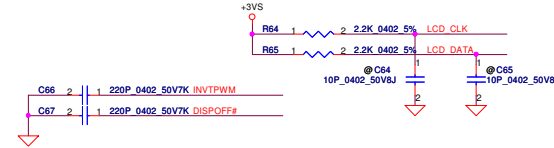
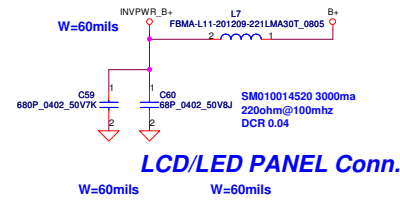
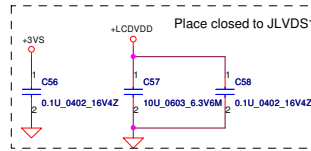
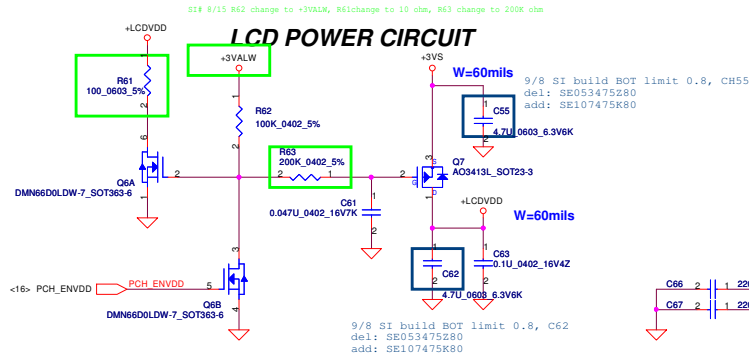
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Issued Date	2011/06/29	Deciphered Date	2011/06/29	MiniCard & WLAN	
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				Date:	Friday, March 02, 2012
				Sheet	31 of 58

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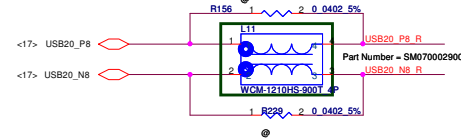
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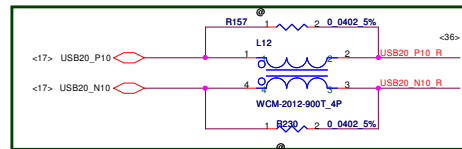
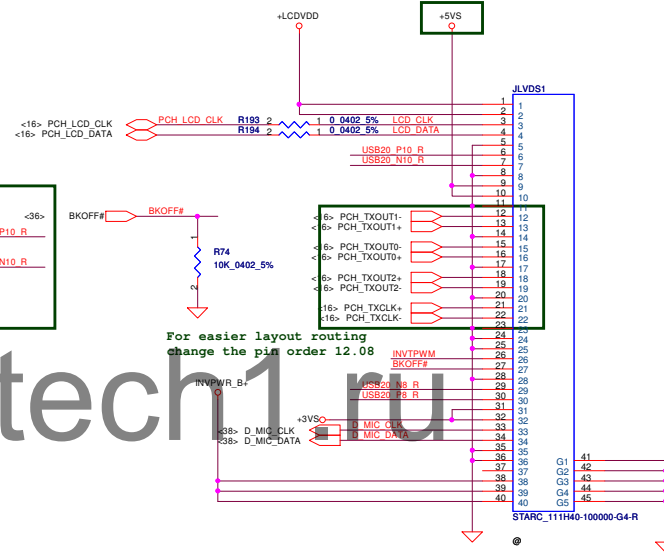
# LCD POWER CIRCUIT



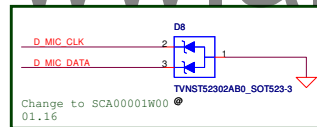
Change to smaller package  
01.16



+3VS& +5VS for touch screen (choose one when getting spec) 12.09

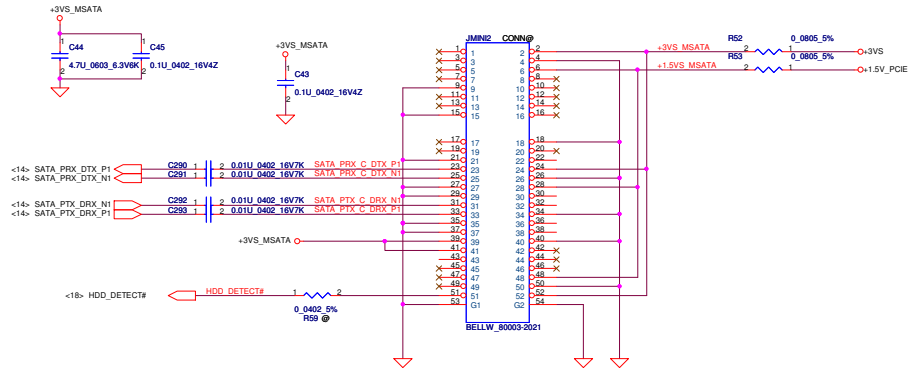


Port 10 for touch screen  
12.07



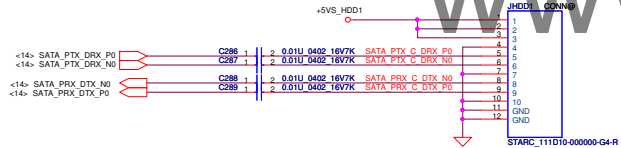
Security Classification	Compal Secret Data		Title	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Size
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				0.1
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mSATA Conn.

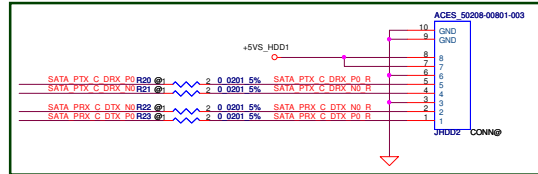
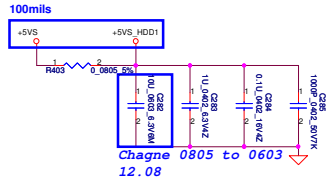


Exchange port 0 & port 1 for SI as customer request  
11.30

Change footprint to Starconn (PAD is bigger)  
11.30



SATA connector



Co-layout for wire type connector

01.16

Change connector to ACES\_50376

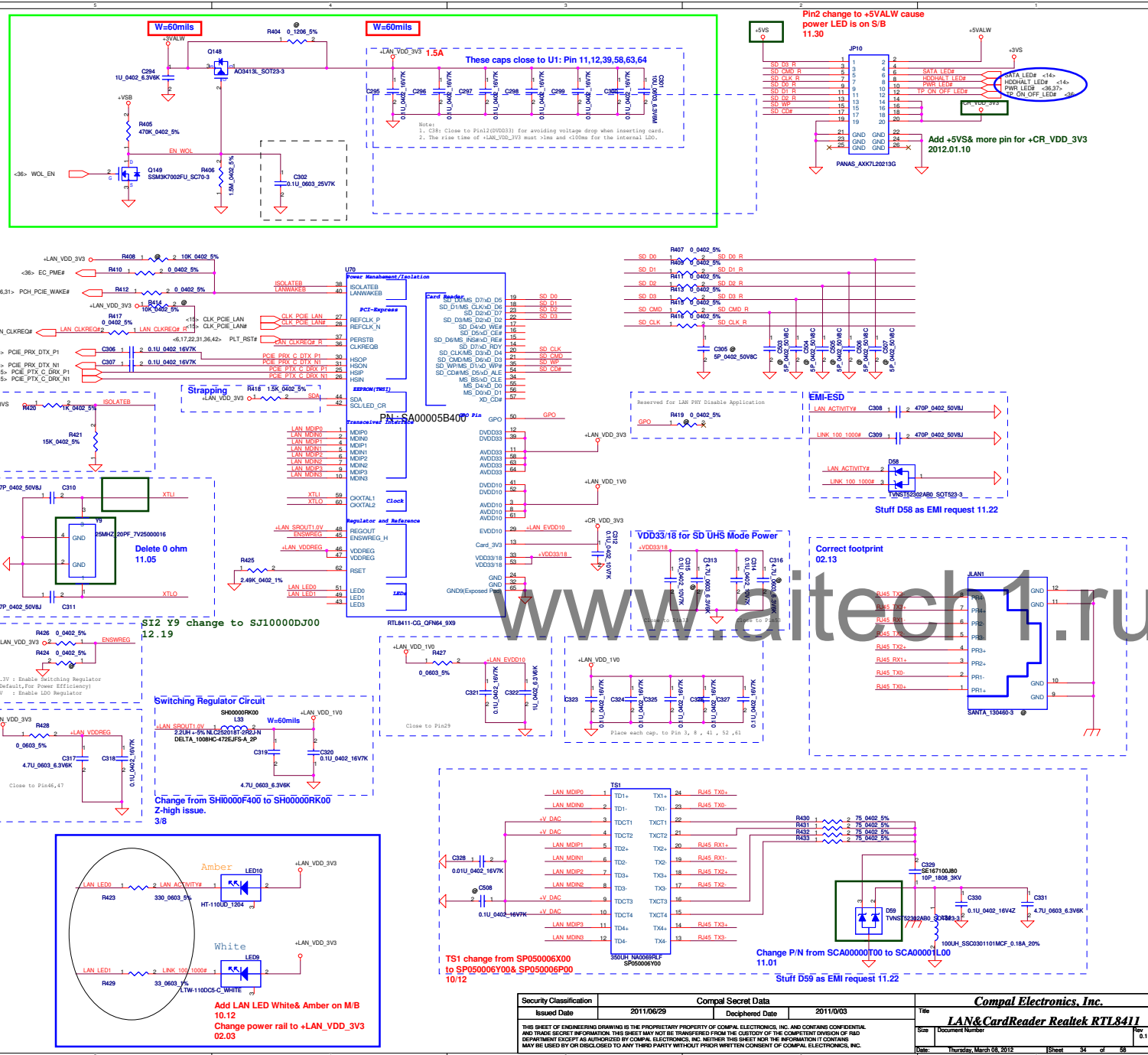
01.31

Change connector to ACES\_50208 because current limit issue

02.06

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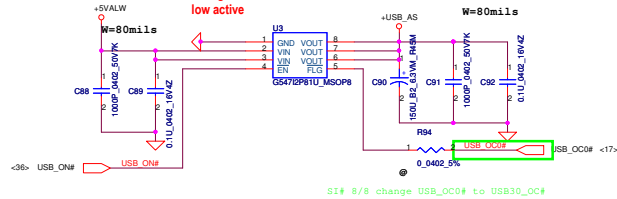




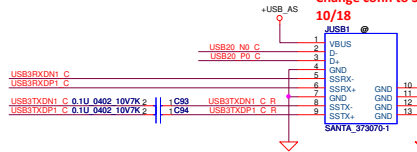
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Issued Date	2011/06/29	Deciphered Date	2011/0/03	LAN&CardReader Realtek RTL8411
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## USB3.0

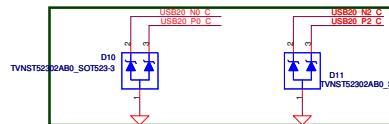
USB3.0 need support 2.5A  
change USB PWR SW SA00003TV00  
low active



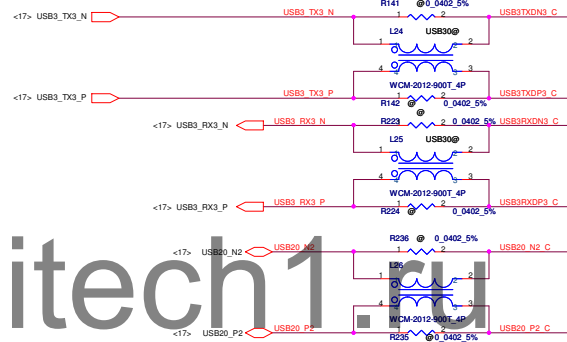
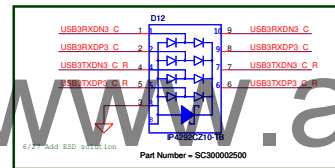
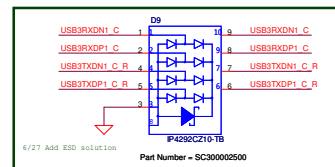
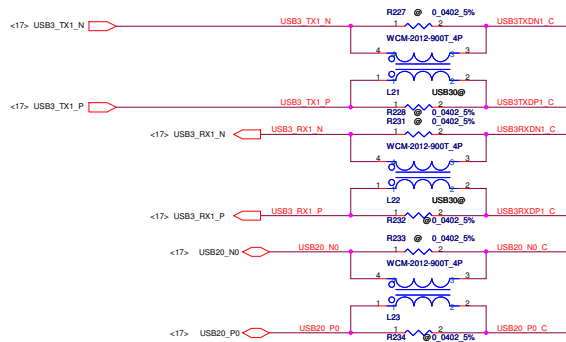
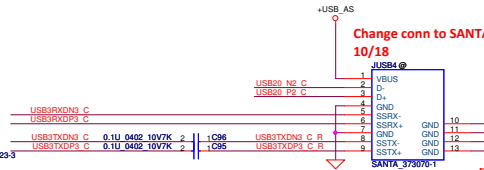
Change conn to SANTA-373070  
10/18



Change P/N from SCA00001T00 to SCA00001L00  
11.01  
Change P/N to SCA00001W00 for smaller size, 10\*10 choke  
02.13

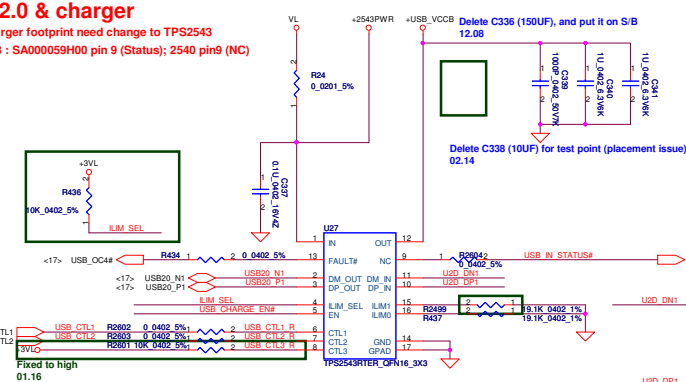


Change conn to SANTA-373070  
10/18

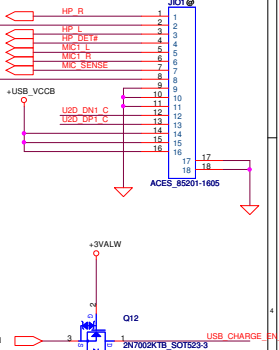
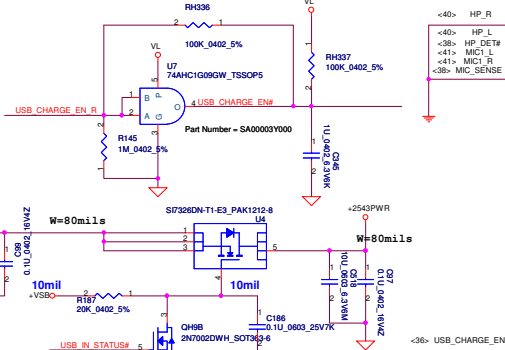
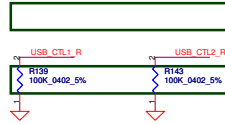


## USB2.0 & charger

USB charger footprint need change to TPS2543  
TPS2543 : SA000059H00 pin 9 (Status); 2540 pin9 (NC)



Delete pull-high resistors  
01.16

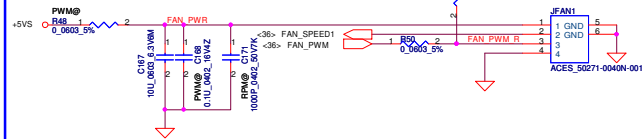
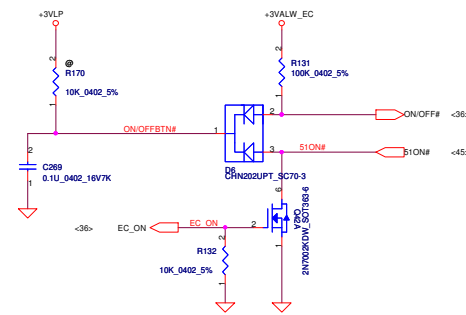


Follow EMI request add choke  
11.08

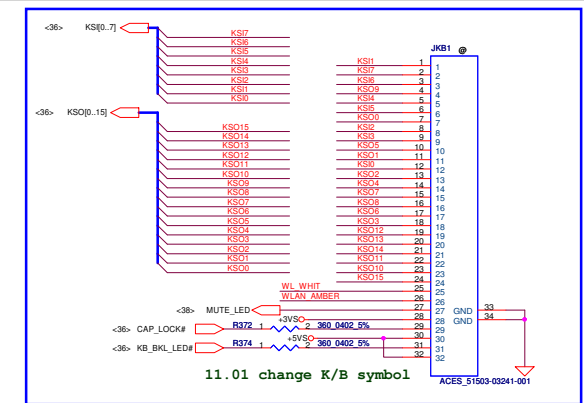
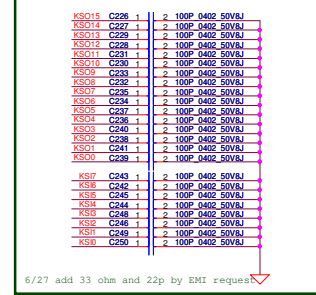
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	USB Con & Daughter Con
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Date	Monday, March 05, 2012	Sheet	35	of	58



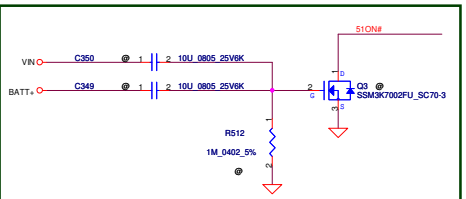
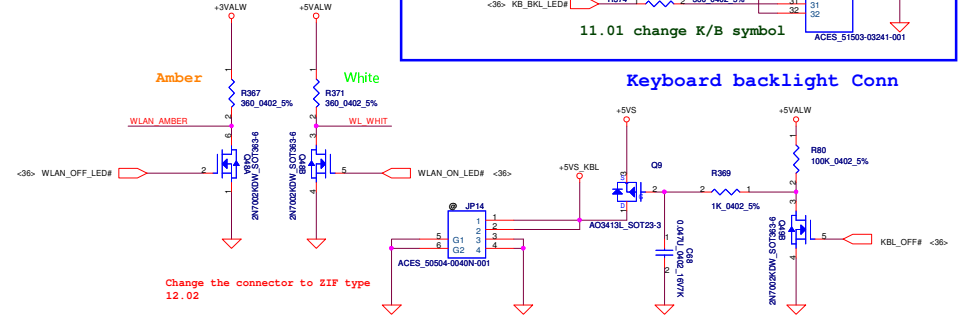
### PWM Fan Control circuit



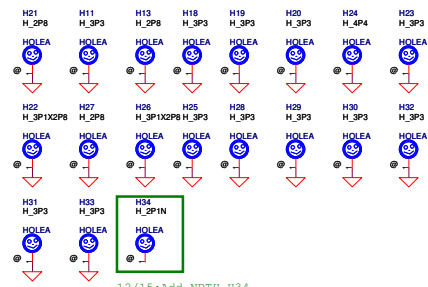
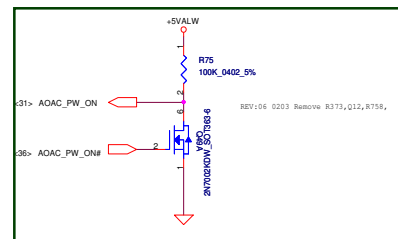
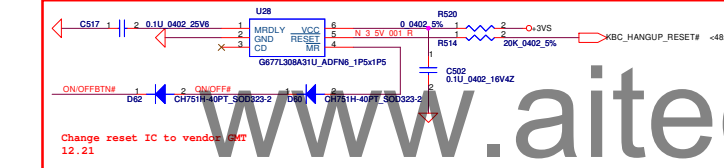
**Follow thermal (FAN) design guide, pull-high 10K**  
12.05



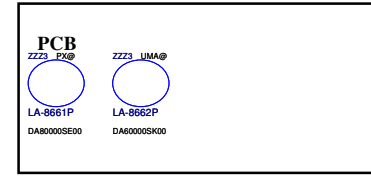
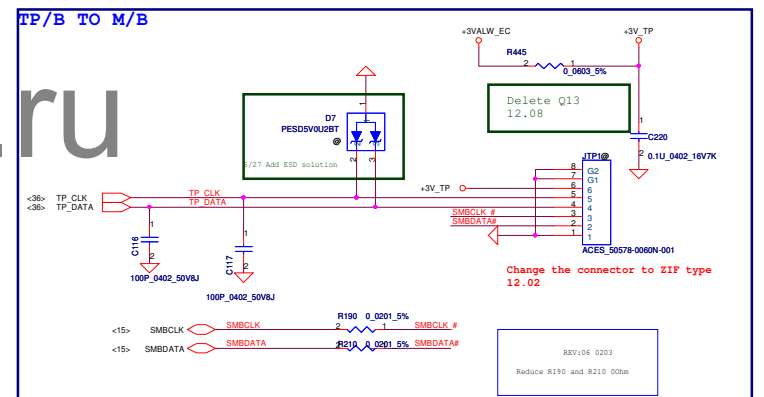
Keyboard backlight Conn



Add C49 as EMI request.  
12.05



12/15: Add NPTH H34



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				Date	Saturday, March 03, 2012
				Isort	37 of 58

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DVDD\_IO should match  
with HDA Bus level(optional for 3.3V signaling or 1.5V signaling)

**Follow EMI request, reserve cap**  
**11.03**

**Correct CA508 circuitry.**  
12.05

**Follow EMI request, reserve cap.**  
**11.03**

**SB Beep**

If Sense\_A total length is greater than  
6 inches, change C12 to 0.1uF

If Sense\_B is un-used, then pull high  
Sense\_B to AVDD by 10Kohm resistor

Ext MIC

Internal SPKR(front stereo speaker

Place C209,C210,CA87,CA89 close to Codes

W=40Mil

+5VS

VIN

VOUT

EN

BYPASS

GND

+VDDA CODEC

CA100  
0.1u 0402\_25V6

CA19  
0.1u 0402\_25V6

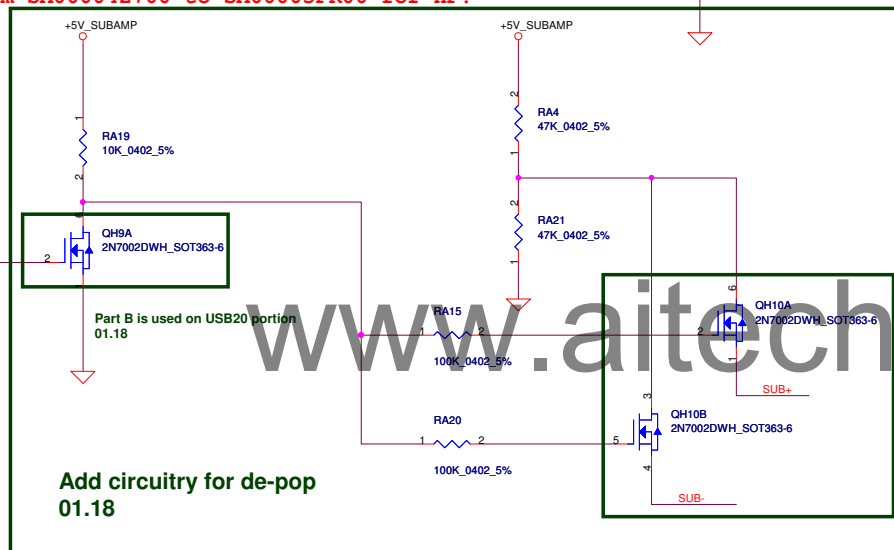
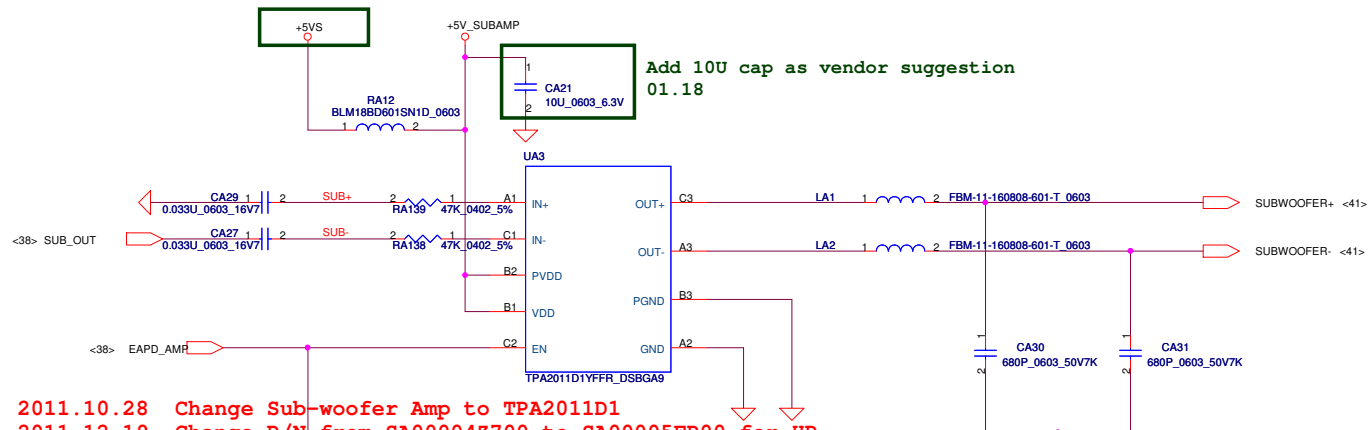
10K\_0402\_5%

IP S78347/50BVR\_S0T23-5

Change UA2 P/N to SA00005J000 just for HP project.  
02.06

**Change UA2 P/N to SA00005J000 just for HP project.**  
02.06

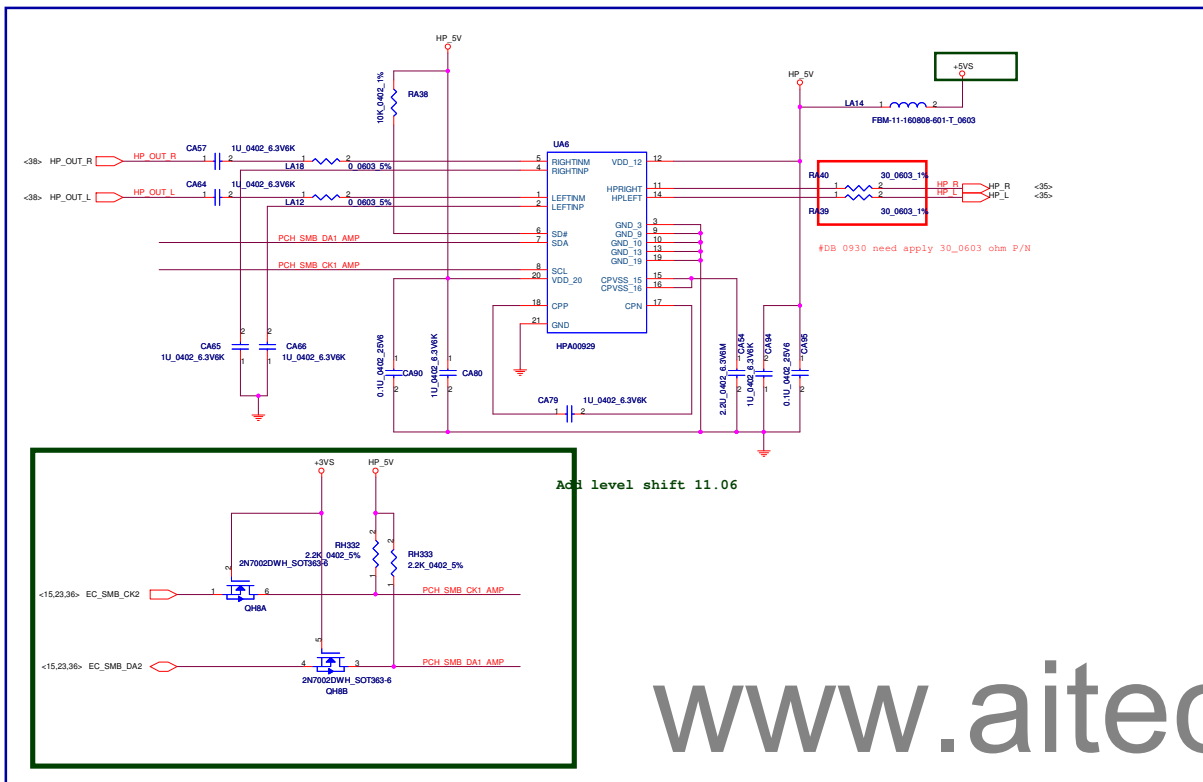
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			Date Friday, March 02, 2012	Sheet 16 of 58



QH10 must change to BJT before SMT  
(Footprint is compatible from BJT & MOTFET)  
01.18  
BJT P/N: SB00000VH00

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				Size B	Document Number		Rev 0.1	
				Date:	Friday, March 02, 2012		Sheet	39 of 58

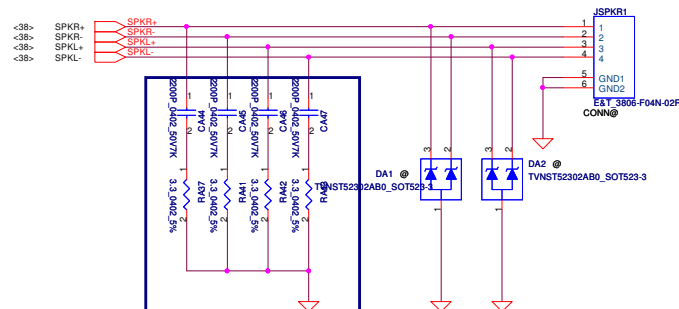
## Headphone amplifier



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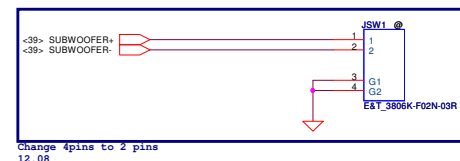
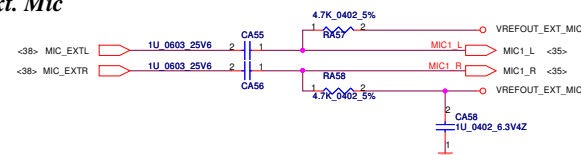


# Front Speaker Connector 1



Need place rear Audio Codec (UA5)

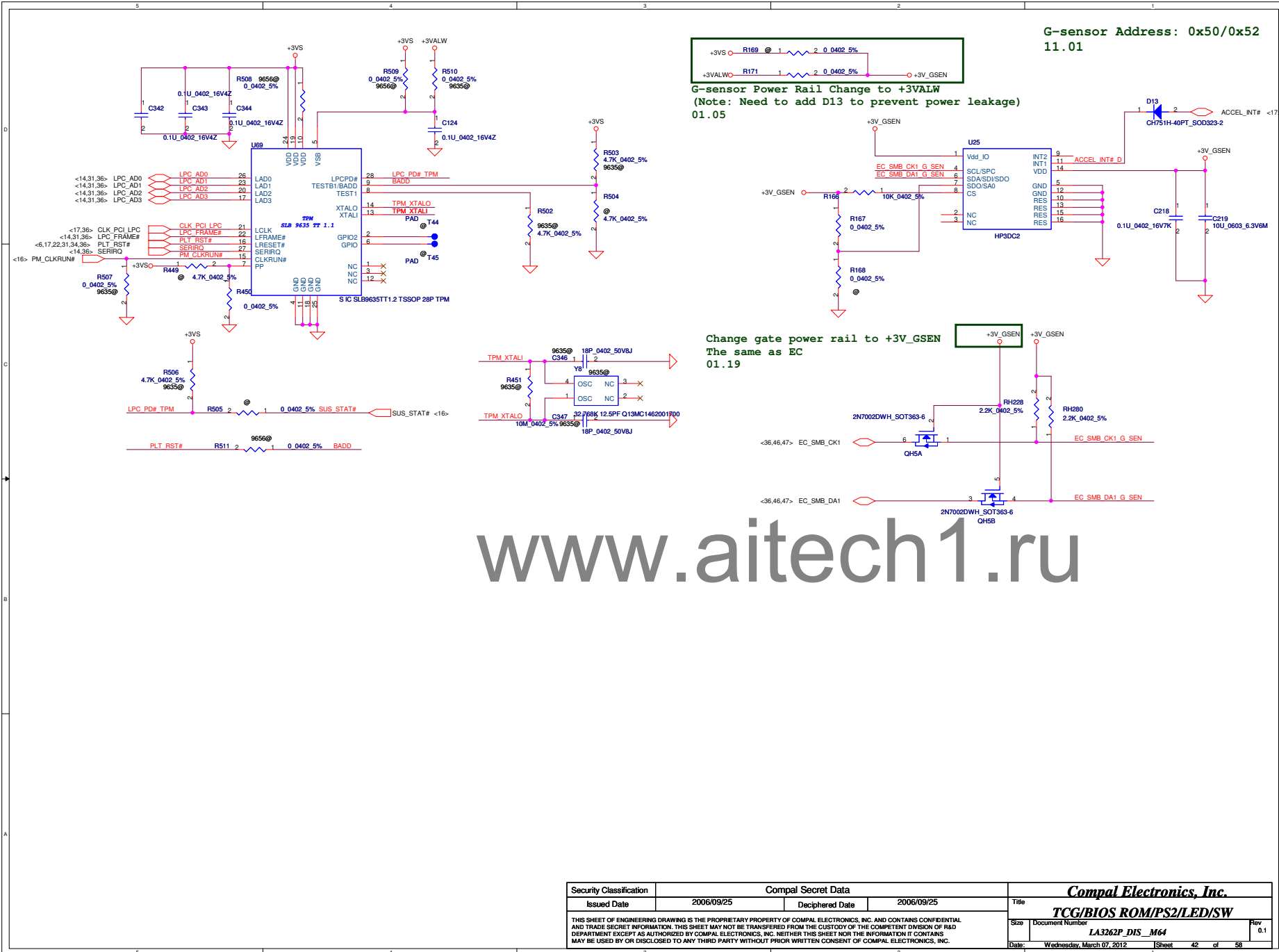
# Ext. Mic



Change 4pins to 2 pins  
12.08

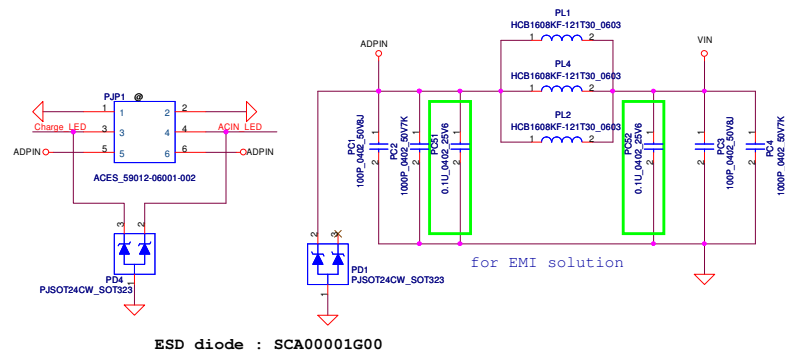
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Issued Date	2009/04/07	Deciphered Date	2012/10/21	Title Audio SPK Conn/Jack/MIC	
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				Date Friday, March 02, 2012	Rev 0.1
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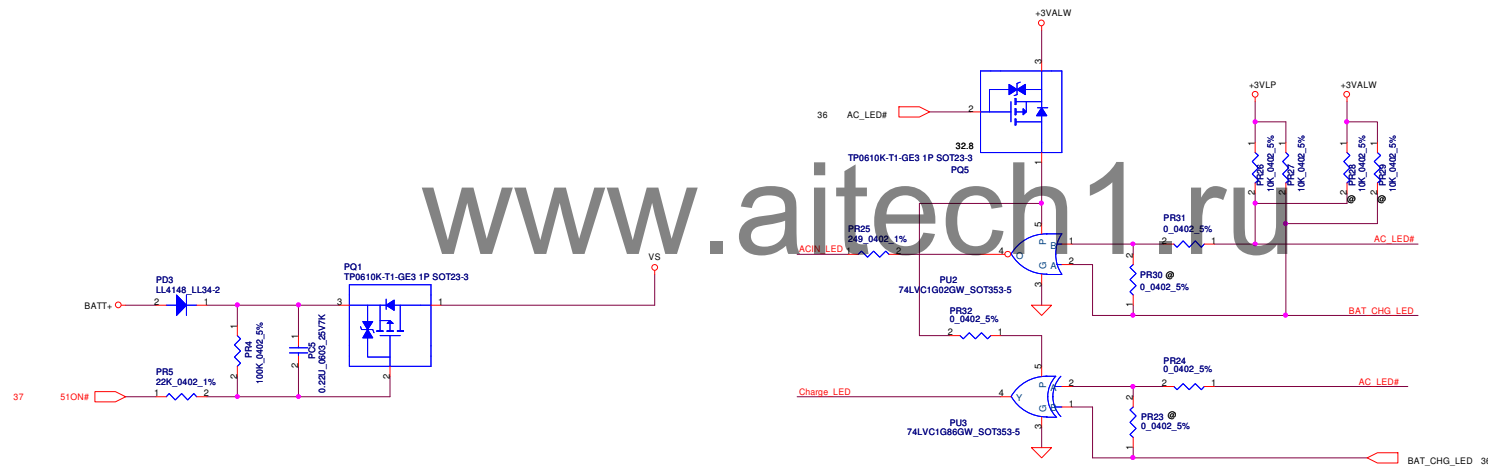


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				Cushman LA-8661P	0.1
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	QAZ60 Strap pin Table		@:un_install	
	Netname	setting	BOM config	
CPU	CFG2	1	RC40 @	1: Normal Operation; Lane # definition matchessocket pin map definition 0: Lane Reversed
	CFG4	1	RC41 @	1 : Disabled; No Physical Display Portattached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
	CFG[6:5]	0 1	RC49 RC48 @	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
	CFG7	1	RC50 @	1: (Default) PEG Train immediately following xRESETB de assertion 0: PEG Wait for BIOS for training
PCH	PCH_INTVRMEN	H	RH124 RH126 @	H : Integrated VRM enable L : Integrated VRM disable
	HDA_SPKR	L	RH139 @	H:No Reboot L:Default
	HDA_SYNC	H	RH149	This signal has a weak internal pull-downOn Die PLL VR is supplied by H:1.5V when smapled high L:1.8V when sampled low Needs to be pulled High for Huron River platfrom
	HDA_SDOUT	L	RH140 @	ME debug mode , this signal has a weak internal PD L=>security measures defined in the Flash Descriptor will be in effect (default) H=>Flash Descriptor Security will be overridden
	DSWODVREN	H	RH213 RH215 @	On Die DSW VR Enable H : Enable L : Disable
	SLP_ME_CSW_DEV#	H	RH267 RH241 @	On-Die PLL Voltage Regulator This signal has a weak internal pull up H : On-Die voltage regulator enable L : On-Die PLL Voltage Regulator disable
	PCH_GPIO37	L	RH245 @ RH246	FDI TERMINATION VOLTAGE OVERRIDE L: Tx, Rx terminated to same voltage(DC Coupling Mode)
	GPIO27	H	RH250 @	PCH_GPIO27 (Have internal Pull-High) H: VCCVRM VR Enable L: VCCVRM VR Disable

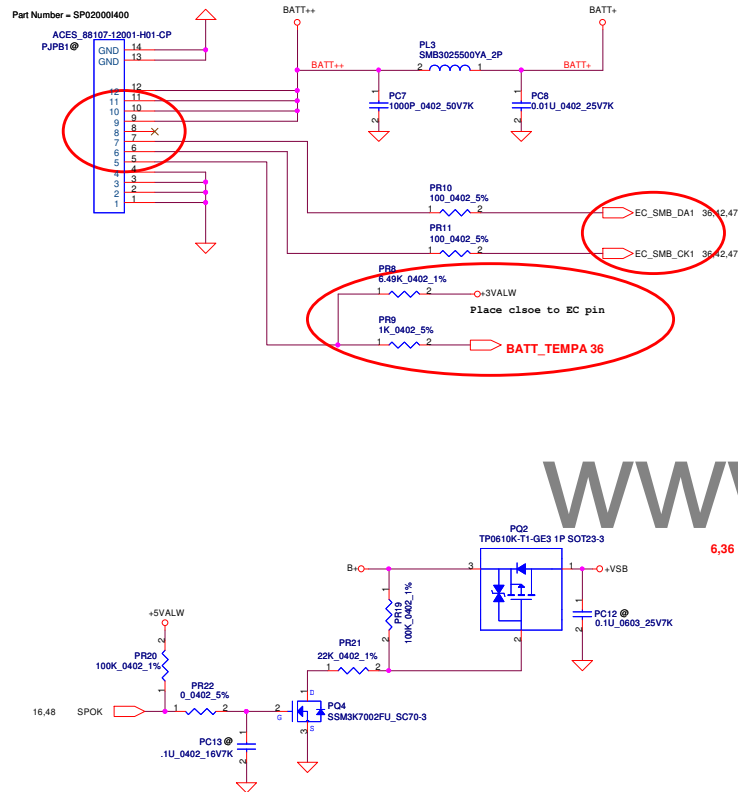


KBC output		Input to Battery		
AC_LED#	BAT_CHG_LED	ACIN_LED	Charge_LED	LED Status
0	0	1	0	White LED light
0	1	0	1	Amber LED light
1	0	0	0	X (don't care)
1	1	0	0	X (don't care)



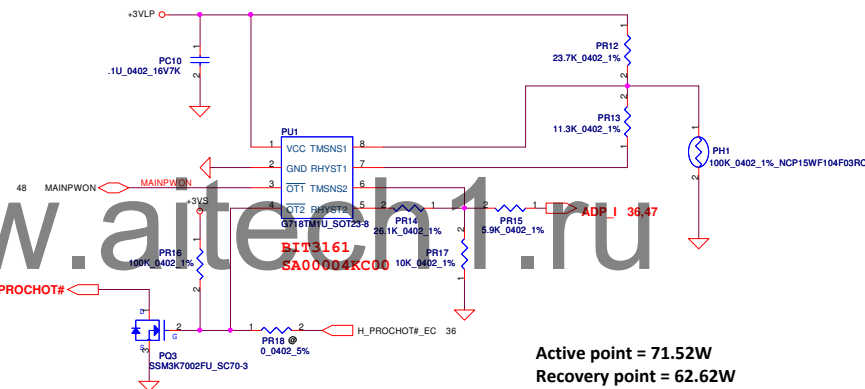
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For KB930 --> Keep PU1 circuit  
(Vth = 0.825V)



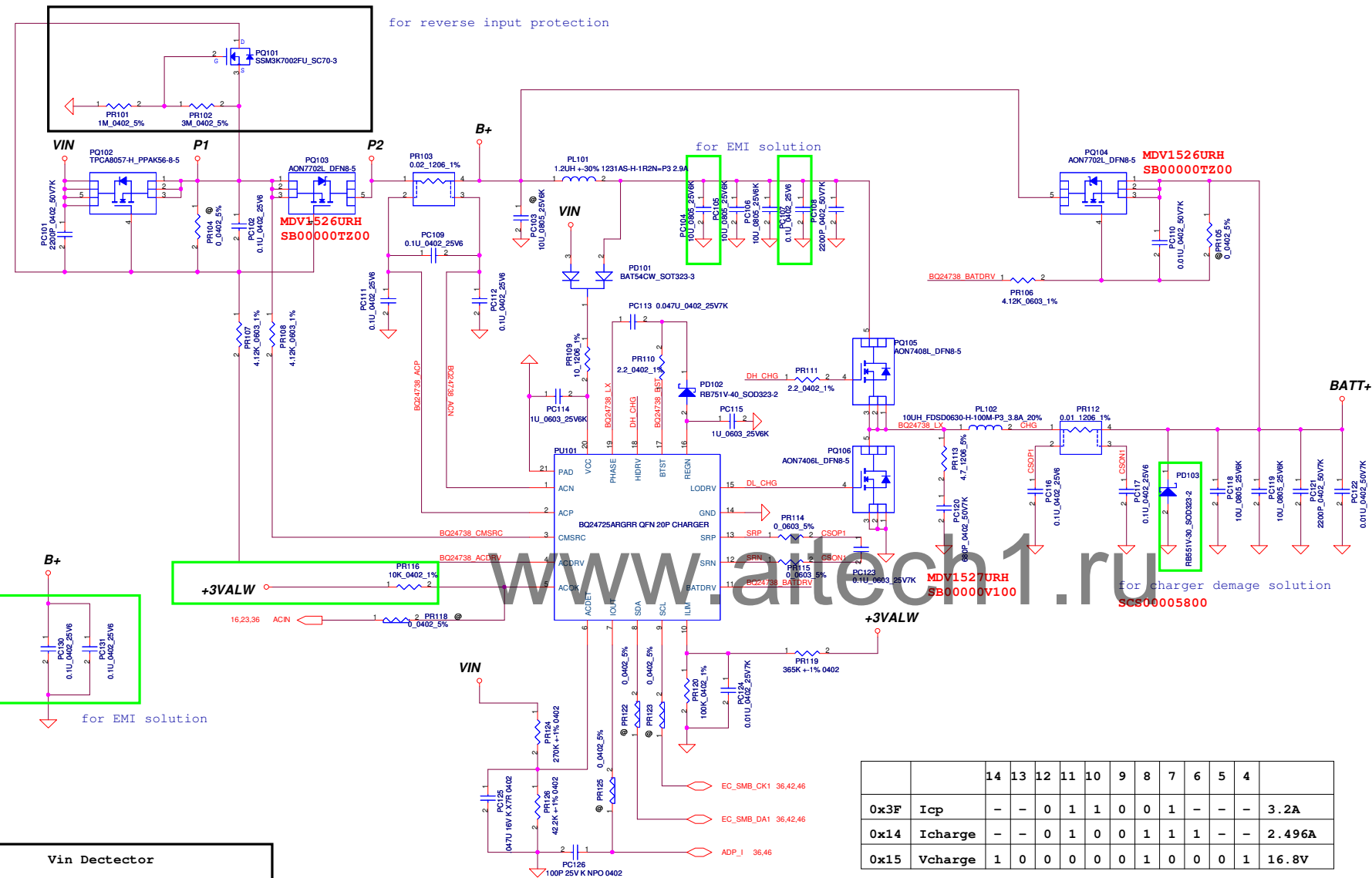
PH1 under CPU bottom side :  
CPU thermal protection at 90 +3 degree C  
Recovery at 56 +3 degree C

Rset = 3 \* Rtmh  
Rhyst = (Rset \* Rtml) / (3 \* Rtml - Rset)  
Rtmh at 90C = 7.8K, Rtml at 56C = 26.1K  
Rset = 3 \* 7.8K = 23.4K ==> 23.7K  
Rhyst = (23.4K \* 26.1K) / (3 \* 26.1K - 23.4K) = 11.12K ==> 11.3K



Active point = 71.52W  
Recovery point = 62.62W

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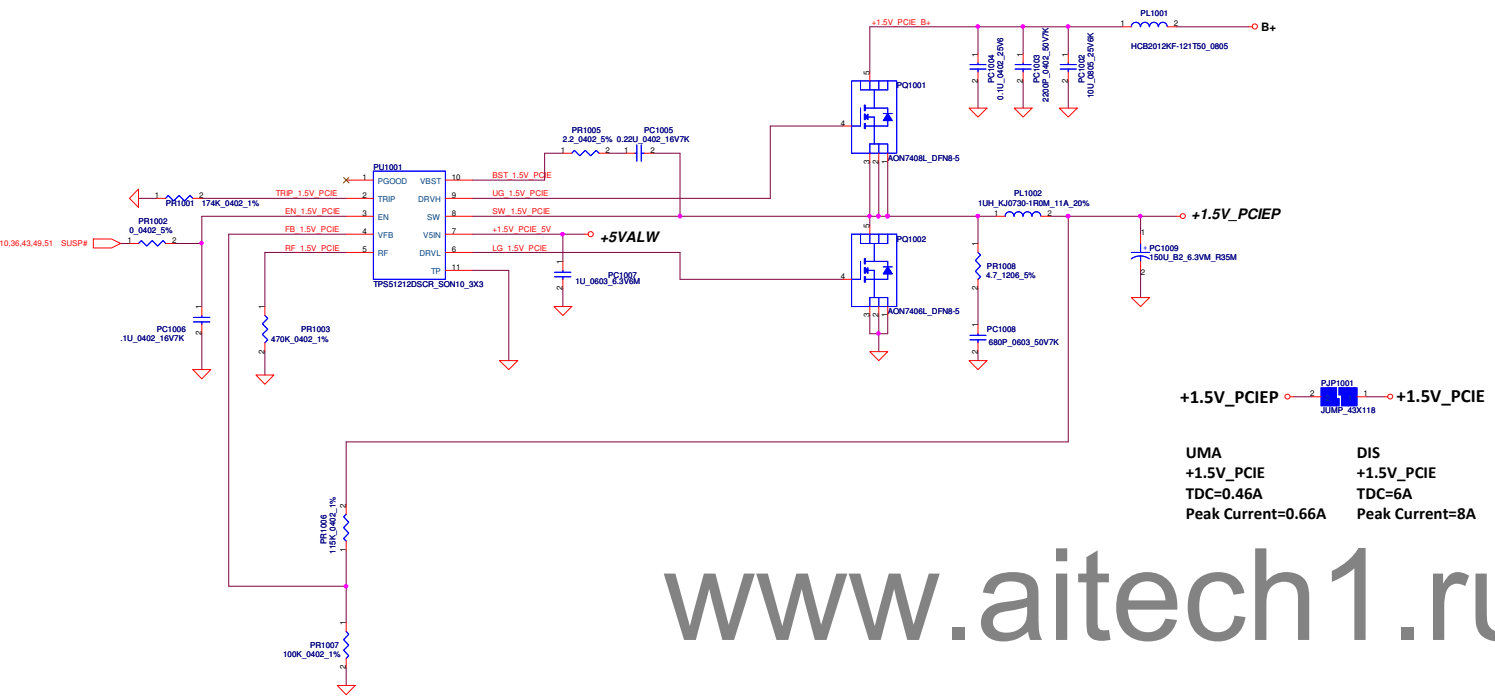
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2011/10/03		2014/12/31		Compal Electronics, Inc.	
2014/12/31		Title		PWR- CHARGER	
Size		Document Number		LA-8551P	
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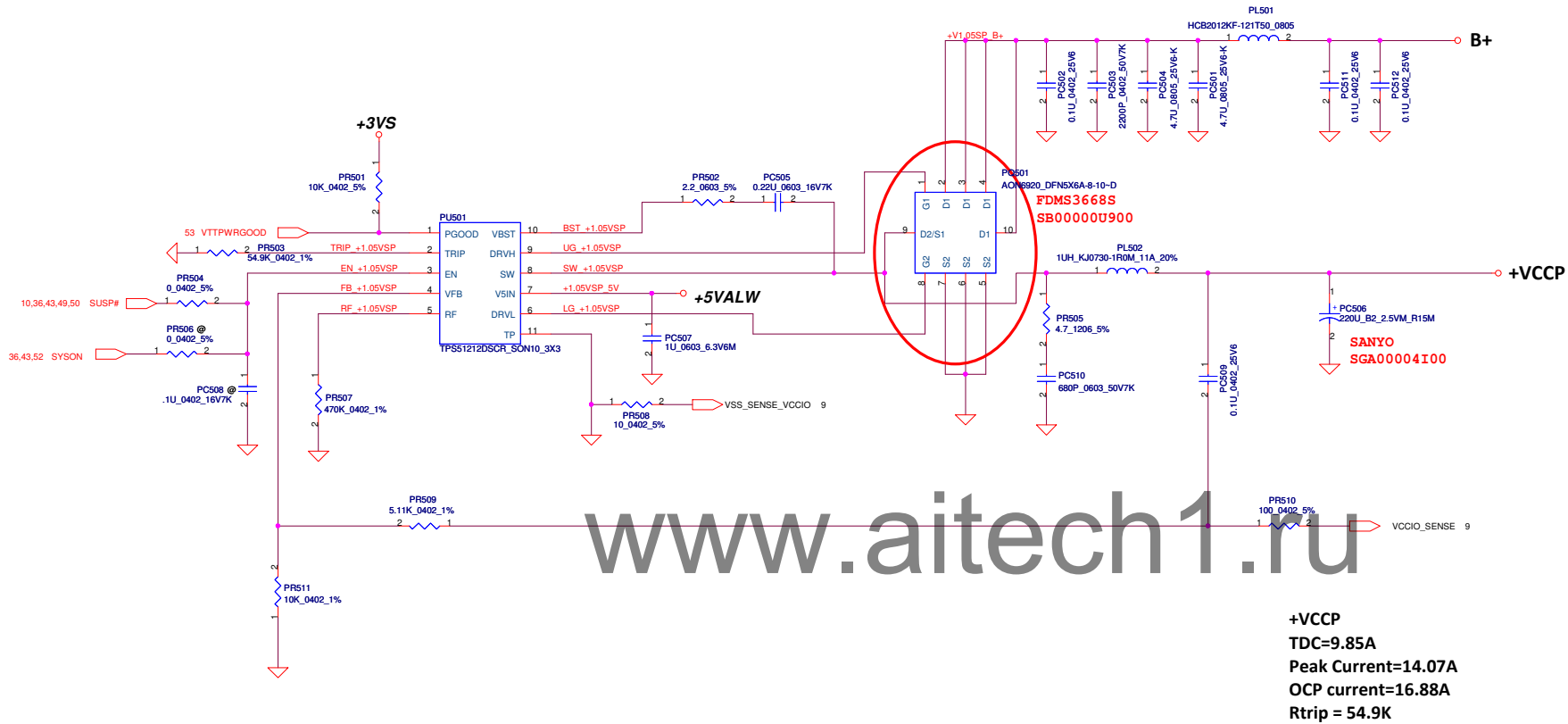


UMA  
+1.5V\_PCIE  
TDC=0.46A  
Peak Current=0.66A

DIS  
+1.5V\_PCIE  
TDC=6A  
Peak Current=8A

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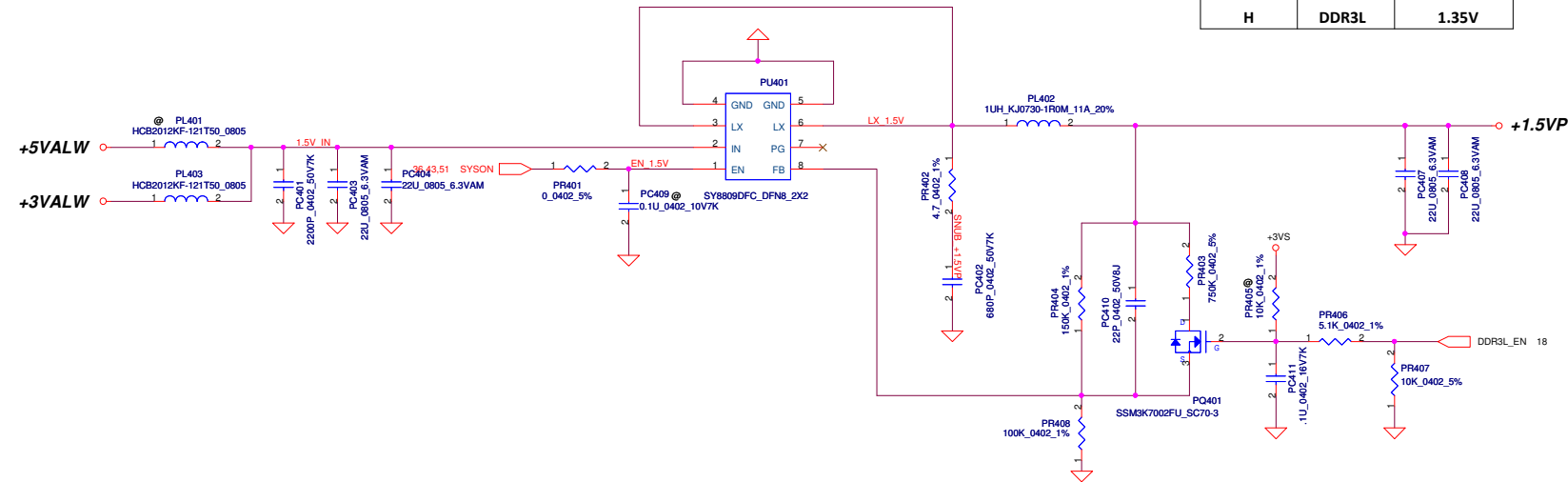


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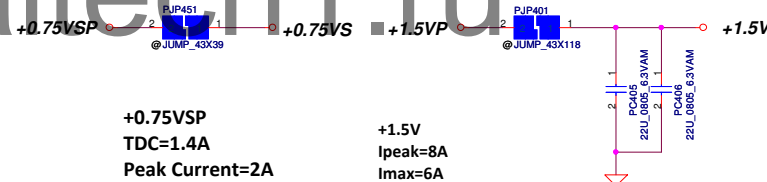
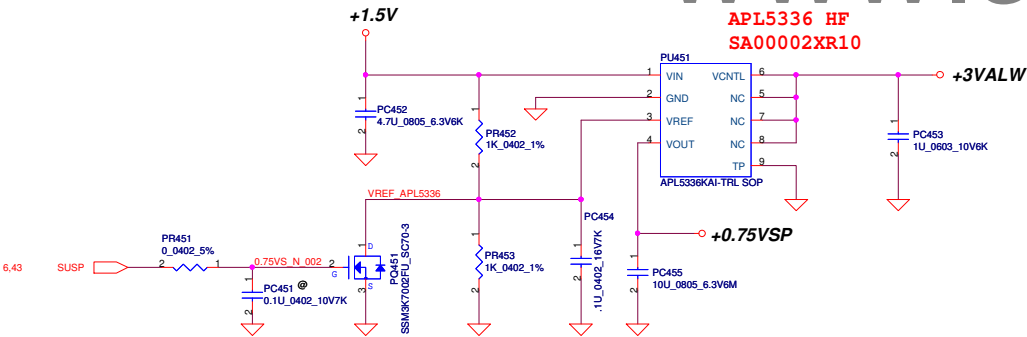
+VCCP  
TDC=9.85A  
Peak Current=14.07A  
OCP current=16.88A  
Rtrip = 54.9K

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DDR3L_EN		1.5VP
L	DDR3	1.5V
H	DDR3L	1.35V



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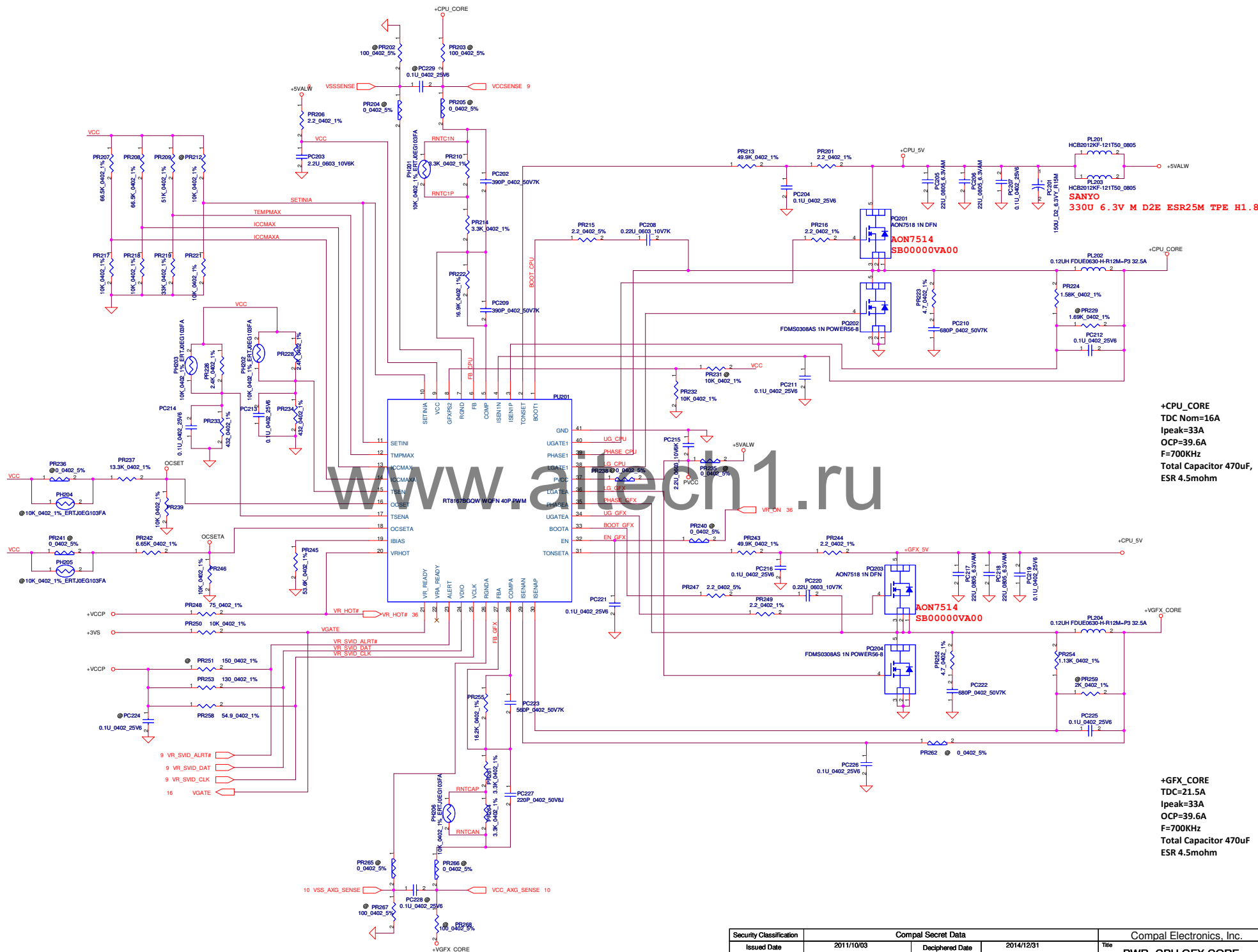


+1.5V  
Ipeak=8A  
Imax=6A  
Total Capacitor 1050uF,  
ESR 4.43mohm

HW side:  
C106 330uF 17m  
C218 390uF 10m  
VGA@ CV122 390uF 10m  
@ C189 330uF 15m

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Size	Document Number	Rev		
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+CPU\_CORE  
TDC Nom=16A  
Ipeak=33A  
OCP=39.6A  
F=700KHz  
Total Capacitor 470uF,  
ESR 4.5mohm

+GFX\_CORE  
TDC=21.5A  
Ipeak=33A  
OCP=39.6A  
F=700KHz  
Total Capacitor 470uF  
ESR 4.5mohm

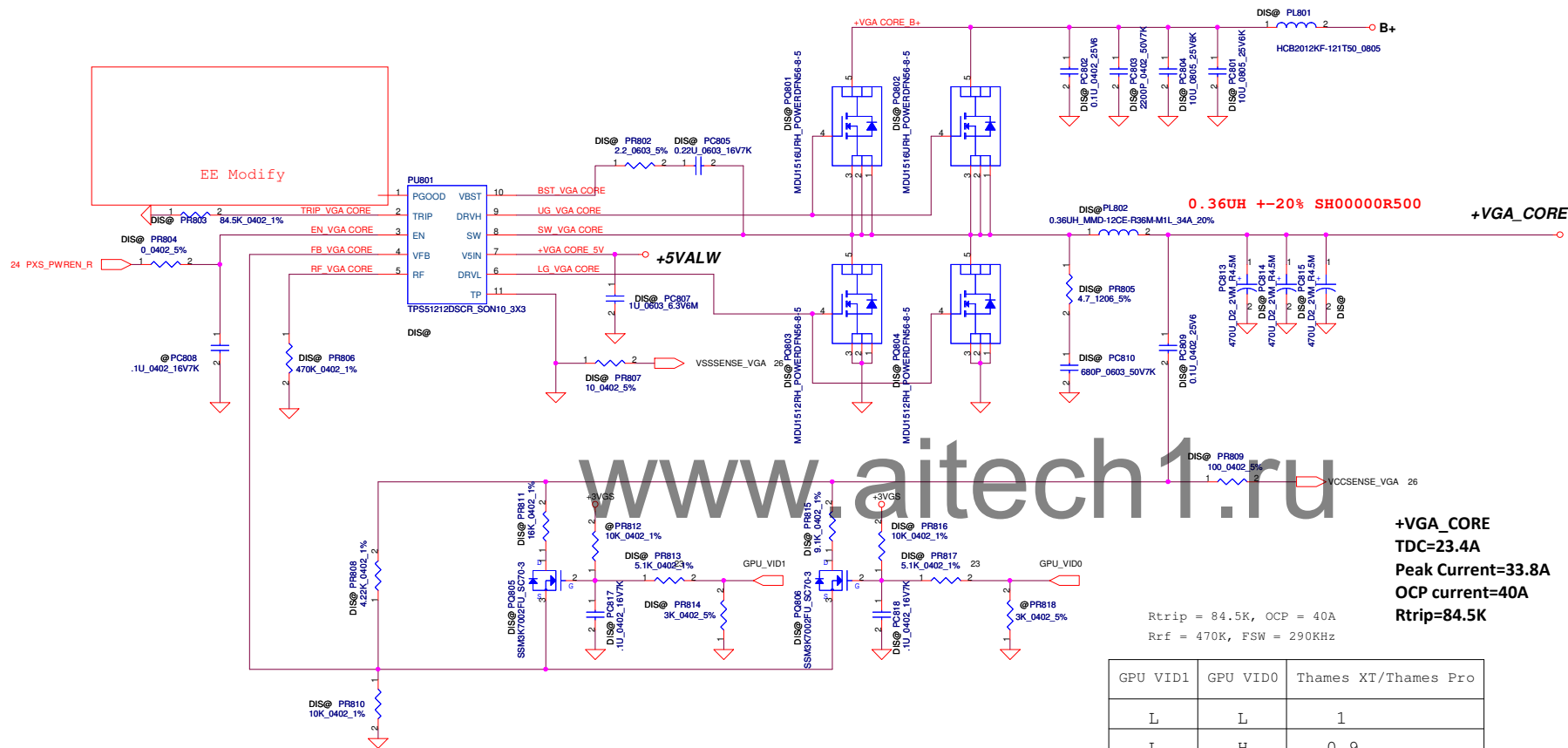
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**+VGA\_CORE**  
**TDC=23.4A**  
**Peak Current=33.8A**  
**OCP current=40A**  
**Rtrip=84.5K**

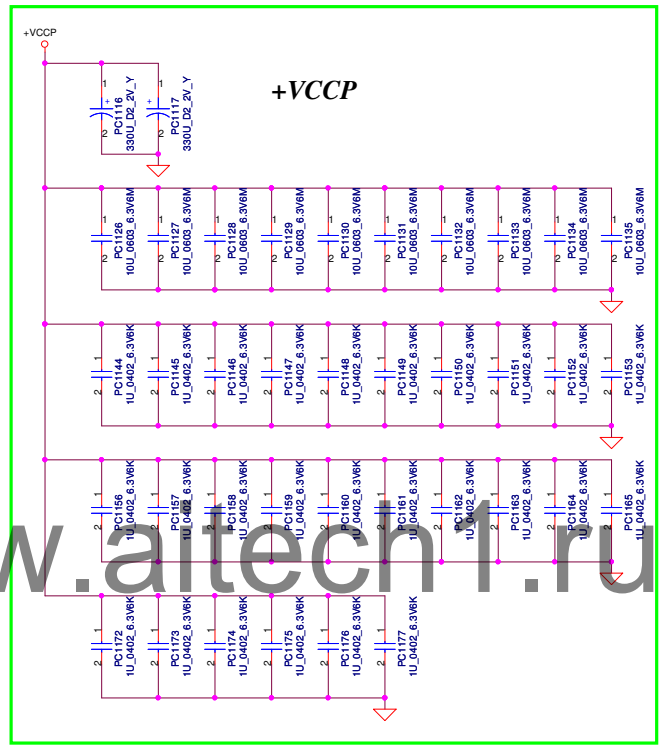
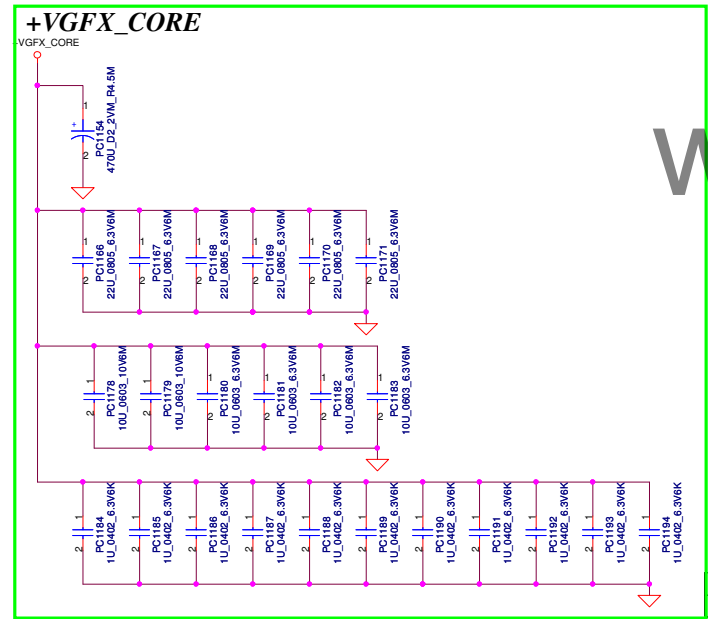
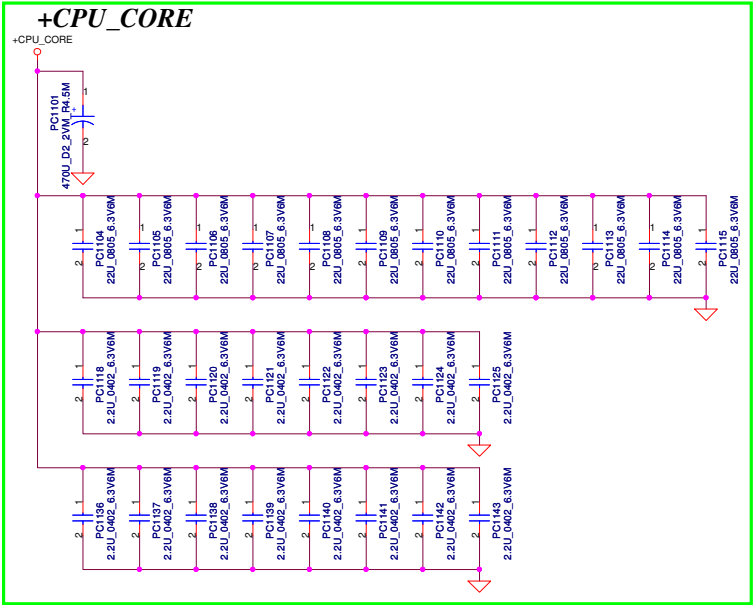
Rtrip = 84.5K, OCP = 40A  
 Rrf = 470K, FSW = 290KHz

GPU VID1	GPU VID0	Thames XT/Thames Pro
L	L	1
L	H	0.9
H	L	0.94
H	H	0.875

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				PWR - PROCESSOR DECOUPLING	
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	change PC111 to 0402	2011/11/28		For layout space		
2	47	remove PR121	2011/11/28		0ohm, not needed		
3	47	change PR124 to 270K, PR126 to 42.2K	2011/11/28		change Vin detector setting		
4	47	change PC125 to 0.047uF	2011/11/28				
5	47	change PR125 to 0ohm, PC126 to 100pF	2011/11/28		FAE review recommand		
6	47	change PR119 to 365K	2011/11/28		modify charge Ilimit to 3.54A		
7	47	change PR111 to 0ohm	2011/11/28				
8	47	add PL101	2011/11/28				
9	46	delete PD5, PD6	2011/11/28		imbedded battery, ESD diode is not needed		
10	46	SMC, SMD exchange	2011/11/28				
11	46	delete pin8 and pin5, add battery temp sense at pin5.	2011/11/28		EC request to need one detect pin if SMB communication fail.		
12	47	change PQ302 to AON7518	2011/11/28				
13	50, 52	change PU1001, PU401 from SY8036HDBC to SY8036LDB	2011/11/28				
14	53	change PU651 from SY8037DCC to SY8037ADCC	2011/11/28				
15	52	add PQ401, PR406, PR407, PC411	2011/11/28				
16	56	change PR1055 to 28.7K	2011/11/28		for correct 1.0V voltage		
17	54	change PL202, PL204 to SH00000PP00, 0.12uH	2011/11/28				
18	54	change PU201 to RT8167, SA00005AU00	2011/11/28				
19	54	change PQ201, PQ203 to AON7518, SB00000U300	2011/11/28				
20	54	change PQ202, PQ204 to FDMS0308AS, SB00000U400	2011/11/28				
21	55	change PL802 to 0.36uH, SH00000HD00	2011/11/28				
22	52	change PU401 to SY8809DFC	2011/11/29				
23	45, 48	change PD2, PD301 DIO CD4148WN-1 1206	2011/11/29		For cost and layout space		
24	51	add PC511, PC512	2011/12/11				
25	54	change PL201 to 0805, and add PL203	2011/12/11				
26	48	add PR320	2011/12/11		tune frequency		
27	55	change PC813, PC814, PC815, PC816 tp 330uF 9m	2011/12/11				
28	47	change PQ101 to SB000009610	2011/12/11				
29	54	change PR210, PR214, PR261, PR264 to 3.3K; PR222 to 15.8K; PR255 to 10.5K; PC202, PC209 to 270p; PC223 to 220p; PC227 to 560p; PR224, PR254 to 1.82K; PR207 to 127K	2011/12/11		First tune CPU, GFX transient		
30	47, 54	change PR111, PR110, PR216, PR249 to 2.2 ohm	2011/12/12		For EMI solution		
31	53, 56	change PL602, PL1052 to SH00000MM00	2011/12/12		For crack issue		
32	55	change PL802 to SH00000HQ00	2011/12/12		For thermal solution		
33	48	change PL303 to SH00000CN00	2011/12/12		For thermal solution		
34	47	change PR114, PR115 to 0 ohm	2011/12/14		Prevent charger damaged by negative output voltage		
35	54	change PR207 to 66.5K	2011/12/14		For GFX GT2 current limit		
36	54	change PR237 to 23.7K +-1% 0402	2011/12/23				
37	54	change PR241 to 1/16W 0 +-5% 0402	2011/12/23				
38	54	change PR242 to 23.7K +-1% 0402	2011/12/23				
39	47	change PQ103, PQ104 to SB00000TZ00	2011/12/23				
40	47, 48	change PQ106, PQ303 to SB00000H700	2011/12/23				
41	54	change PR210, PR261, PR264 to 3.3K +-1% 0402	2011/12/23				
42	53	change PL651 to SY8037CDCC	2012/1/11		For latch mode		
43	57	change PC1180, PC1181, PC1182, PC1183 to SE000005T80	2012/1/11		For height limit		
44	46	Delete PC11	2012/1/12		For ME request		

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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
45	47	change PR114 to 10, PR115 to 6.8ohm, add PD103	2012/1/30		For Charger issue		
46	47	Add PC130, PC131, PC104, PC107	2012/1/30		For EMI solution		
47	48	Add PR321	2012/1/30		Choose working frequency to improve efficiency and thermal		
48	50	change 1.5VPCIE Circuit	2012/1/30		Change input voltage form 5V to 19V to slove thermal issue		
49	52	Add PL403	2012/1/30		Choose input voltage to slove thermal issue		
50	54	Change PR224 to 1.58Kohm, PC209 to 220PF, PC202 to 390PF, PR222 to 16.9Kohm, PR237 to 21.5K	2012/1/30		Base on SI layout, FAE review recommand value		
51	48	change PL303 to SH00000F600	2012/1/30		For thermal issue		
52	45	Delete PD2, PR2, FR3, PC6	2012/1/30		For Layout space		
53	47, 48, 54	Change PQ302, PQ201, PQ203 to AON7514	2012/1/30		For efficiency		
54	51	Delete PJP501	2012/1/30		For Layout space		
55	55	Change PC813, PC814, PC815 to 470uF, delete PC816 Change PL802 0.36uF to 13*13*3.5 size	2012/1/30		For thermal issue		
56	55	Add PC820, PC821, PC822	2012/1/30		For VGA transient voltage		
57	57	Change PC1180, PC1181, PC1182, PC1183 to SE000005T80	2012/1/30		For ME request		
58	47	change PQ102 to TPCA8057	2012/1/30				
59	54	change PC223 to 560pF, PC227 to 220pF	2012/2/17		For FAE suggesstion		
60	48	change PQ302 to AON7518	2012/2/17		For efficiency		
61	55	change PL802 to 13*13*3 size	2012/2/17		For thermal solution		
62	47	change PR114, PR115 to 0 ohm, PD103 to SCS00005800	2012/2/17		For HP and soucer request		
63	54	change PC201 to 330uF	2012/2/17		For acoustic solution		
64	45	change LED circuit	2012/2/23				
65	48	change PL303 to 3.3uH 10*10*3H, PC313 to 150U_B2_6.3VM_R35M, remove 5V output jumper	2012/2/23		For thermal solution		
66	53	change PU651 to SY8037DDCC	2012/2/23		For UHV CPU and latch mode		
67	55	change FR812 and FR816 power to +3VGS	2012/2/23		For leakage issue		
68	45	change LED circuit	2012/2/29				
69	54	change PC209 to 390pF, PR237 to 13.3Kohm, PR254 to 1.13Kohm, PR255 to 16.2Kohm, PR242 to 6.65Kohm	2012/2/29		Base on PV layout		
70	45	change PL1, PL2 to 0603 size, add PL4	2012/2/29		EMI request		

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